# STUDY OF ALTERNATIVE LOGIC STYLES SUITABLE FOR LOW POWER VLSI DESIGN

**A Thesis Submitted**

**In Partial Fulfilment of the Requirements**

**for the Degree of**

## DOCTOR OF PHILOSOPHY

**in**

**Department of Electronics & Communication Engineering**

**by**

**Neetika Yadav**
**(2K18/PhD/EC/514)**

**Under the Supervision of**

**Prof. Neeta Pandey**
**(Professor, DTU, Delhi)**

**Dr. Deva Nand**
**(Assistant Professor, DTU, Delhi)**


**Department of Electronics & Communication Engineering,**

**DELHI TECHNOLOGICAL UNIVERSITY**
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Main Bawana Road, Delhi-110042, India

**November, 2024**

# CERTIFICATE

This is to certify that the thesis entitled "**STUDY OF ALTERNATIVE LOGIC STYLES SUITABLE FOR LOW POWER VLSI DESIGN"** submitted by Neetika Yadav (2K18/PhD/EC/514) to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi, for the award of the degree of Doctor of Philosophy is based on the original research work carried out by her under our guidance and supervision. In our opinion, the thesis has reached the standards fulfilling the requirement of the regulations relating to the degree. It is further certified that the work presented in this thesis is not submitted to any other university or institution for the award of any other degree or diploma.


**Prof. Neeta Pandey**
Supervisor
Department of Electronics &
Communication Engineering,
Delhi Technological University,
Delhi –110042

**Dr. Deva Nand**
Co-Supervisor
Department of Electronics &
Communication Engineering,
Delhi Technological University,
Delhi –110042

# DECLARATION

I hereby declare that the work presented in this thesis entitled "**STUDY OF ALTERNATIVE LOGIC STYLES SUITABLE FOR LOW POWER VLSI DESIGN"** has been carried out by me under the supervision of **Prof. Neeta Pandey**, Department of Electronics & Communication Engineering, Delhi Technological University, Delhi and **Dr. Deva Nand**, Department of Electronics & Communication Engineering, Delhi Technological University, Delhi and is hereby submitted for the award of the degree of Doctor of Philosophy in Department of Electronics & Communication, Delhi Technological University, Delhi.

I further undertake that the work embodied in this thesis has not been submitted for the award of any other degree or diploma elsewhere.

**Neetika Yadav**

2K18/PhD/EC/514

# ACKNOWLEDGMENT

I extend my deepest gratitude to Prof. Neeta Pandey and Dr. Deva Nand, my esteemed supervisors from Department of Electronics and Communication Engineering (ECE), Delhi Technological University (DTU). Their expert mentorship, constant encouragement, and commitment to academic excellence have indelibly shaped my research's trajectory and quality. The faculty and staff of ECE Department have provided a vibrant academic ecosystem, equipping me with resources and opportunities for intellectual growth. The collaborative spirit within the department and the unwavering support of fellow students have been invaluable.

My colleagues and seniors from the ECE department, particularly Dr. Ranjana Sivaram, Ms. Damyanti, Ms. Sweta, and Ms. Garima, deserve my sincere appreciation for their enduring support.

I am profoundly thankful to my parents and my mother-in-law for their unwavering love and sacrifices that have been my driving force. My husband, Anand, has been an unwavering pillar of encouragement. My siblings' shared experiences have enriched my perspective, and special thanks to my lovely daughter, Zoe, who has displayed remarkable patience during my absence. My family and friends have been my bedrock of support, providing unwavering encouragement and belief during challenging times. While their names may not appear here, their impact on my academic journey is profound. This achievement is a collaborative endeavour, showcasing the contributions of numerous individuals. To all of you, I convey my heartfelt appreciation.

**Neetika Yadav**

# ABSTRACT

In the past decade, technological advancements in Very Large Scale Integration (VLSI) have increased integration density, pushing power to its limits and challenging packaging and cooling systems. The increasing demand for portable devices, notably smartphones, and the expanding adoption of Internet of Things (IoT) necessitate faster, power-efficient devices with extended battery life. As a result, it's crucial to develop energy efficient designs that offer improved performance.

Static CMOS and dynamic domino designs have long dominated the digital arena, yet they have inherent limitations. Static CMOS faces challenges like increased input capacitance, limiting its energy efficiency as fan-in values rise. Dynamic domino design offers lower delay but at the cost of higher energy and sensitivity to process variations. Therefore, balancing power and speed in CMOS gate remain challenging due to energy-delay trade-off.

To overcome these challenges, there is a growing need to search for logic styles and transistor technologies that can act as an alternative to existing CMOS based designs. Additionally, implementing power reduction techniques becomes imperative for these alternative logic styles to have less power. One such alternative logic style is Dual Mode Logic (DML) which offers dual mode functionality, i.e. static mode and dynamic mode, with low power and high speed. However, limited study has been conducted to reduce leakage power in the context of DML circuits. Therefore, leakage reduction techniques i.e. LECTOR and GALEOR are incorporated in footed DML design. Three designs are proposed, namely LECTOR with Dual Mode Logic (LDML), GALEOR with Dual Mode Logic (GDML) and

GALEOR with Dual Mode Logic with footed Diode (GDMLD), to reduce leakage in footed DML design. These designs use the concept of stacking to achieve leakage power reduction.

Other than this, Dual Mode Transmission Gate Diffusion Input (DMTGDI) and Differential Cascode Voltage Switch Logic (DCVSL) are alternative logic styles that can also be explored for Power Delay Product (PDP) reduction. Two such designs- Modified Dual Mode TGDI (M-DMTGDI) and Dual Mode DCVSL (DM-DCVSL) are introduced in this work which offers dual mode functionality along with PDP reduction. In addition to this, the proposed M-DMTGDI design also overcomes the contention issue present in the existing DMTGDI design.

Further the improved transistor technology, primarily Carbon Nanotube Field-Effect Transistor (CNTFET) , can be explored to implement designs, which already exist in MOSFET domain, so as to leverage the benefits of CNTFETs for their implementation. Such designs are put forward in this work, namely, CNTFET based footed DML (C-DML), CNTFET based DMTGDI (C-DMTGDI) and CNTFET based M-DMTGDI (C-MDMTGDI). These designs demonstrate superior performance over their CMOS counterparts, particularly in terms of reducing the PDP. Another area of research that has emerged in CNTFET domain is leakage power. Limited study has been conducted on the implementation of leakage reduction techniques in CNTFETs, using the methods previously developed for MOSFETs. So, for leakage reduction, three leakage reduction techniques namely LECTOR, GALEOR, and LCNT are also proposed for C-MDMTGDI design. Each of these proposed techniques significantly reduces leakage power but at the cost of delay.

In this thesis, the performance of all the proposed designs is analysed and compared with existing counterparts in terms of power, delay and PDP. Functional verification is done

for all proposed designs. The MOSFET based designs are simulated using Symica DE tool and HSPICE tool is used for simulating CNTFET based designs.

# TABLE OF CONTENTS

# LIST OF FIGURES

# LIST OF TABLES

# Chapter 1

# Introduction

## 1.1 Background

Nowadays, the low power designs of complex VLSI circuits are of utmost importance. With each technology generation, the integration density is increasing which is pushing power density and total power consumption to the limits that can be supported by packaging, cooling and other infrastructure [1]. Further, the rise in the demand of portable devices mainly cell phones and the proliferation of mobile applications and IoT solutions require efforts to curb power dissipation to have faster and durable devices with longer battery lifetime without compromising the performance [2]. Therefore, low power designs with improved performance i.e., energy efficient designs are considered essential [3].

Traditionally, static CMOS and dynamic domino designs have dominated the digital design arena for several decades with their respective limitations [4,5]. Large input capacitance and contention issues emerge with increased fan-in values and limits the usage of static CMOS for energy efficient designs [6]. Dynamic domino design offers less delay but at the cost of high energy, increased sensitivity to process variations, charge sharing and charge leakage problems [6,7]. The optimization of CMOS gate is quite challenging due to energy delay trade-off [7].

In order to have optimized designs in-terms of power and delay, efforts have been made to develop logic styles that can act as alternative to static CMOS. Some of the logic styles include Pass Transistor Logic (PTL) [8], Gate Diffusion Input (GDI) [9,10], Differential Cascode Voltage Switch Logic (DCVSL) [11-13], Dual Mode Logic (DML) [14-16], Dual Mode Transmission Gate Diffusion Input (DMTGDI) logic [17,18] and Dual Mode Pass Logic (DMPL) [19] . The PTL style [8] has the advantages of lesser transistor count and delay [8]. The GDI logic style [9] combines CMOS with PTL, and makes

implementation of logic functions simpler. The degradation of full swing at the output in PTL and GDI necessitates usage of additional buffers [9,10]. The DCVSL design provides output in both true and complemented forms. It is available in both static [11] and dynamic configurations [12]. Although the static DCVSL requires more power and is more sophisticated, it has the advantage of reducing parasitic capacitance. Another unique logic style, called DML, allows for flexible switching between static and dynamic operation modes [14]. The DML gates have great performance with marginally more power in the dynamic mode and very low power dissipation and moderate performance in the static mode [15]. As a result, energy efficient designs frequently employ this logic style [15-16].The DML design has also been employed in conjunction with other logic styles- GDI and PTL in [17-19]. In DMTGDI, dual mode operation is made possible by an extra transistor (pre-charge/pre-discharge transistor) positioned between the output node and the supply voltage or ground [17]. Transmission Gate Diffusion Input (TGDI) logic is used to construct the logic in DMTGDI. This variation, like DML, utilises a mode signal to accommodate both static and dynamic operating modes [17]. In DMPL, a PTL network and an extra transistor are employed to realise a function with dual mode operation [19]. Using a mode signal, similar to DML, the DMPL-based designs can operate in static and dynamic mode [19].

The work has also been done to search for improved transistor technology that can lead to design with low power and high performance. Few of such technologies are- Fully Depleted Silicon On Insulator (FDSOI) [20-26], Fin Field-Effect Transistor (FinFET) [27-35], Carbon Nanotube Field-Effect Transistor (CNTFET) [36-48]. Recently, CNTFETs has gained popularity in digital domain mainly for low power designs. The CNTFET provides alternate channel material for transistors, which makes them faster and power efficient as

compared to bulk silicon transistors [36-40]. Presence of 1-D ballistic transport of charge carriers in CNTFETs has resulted in a high mobility and large drive current [39,40]. Also, these devices have large ON current ($I_{on}$), higher $I_{on}/I_{off}$ ratio and provide a unique property to control threshold voltage by simply changing the chiral indices or the diameter of the Carbon Nano Tube (CNT) [39,40].

## 1.2 Available Literature and Scope of Work

Substantial work has already been done by researchers in the quest for search of ways to reduce power in standard CMOS designs and at the same time, search for energy efficient logic styles and improved transistor technology based designs that can act as alternative to conventional CMOS designs. The existing literature can be classified into three main categories:

### 1.2.1 State of the art- Power reduction in standard CMOS designs

Power can be divided mainly into two types- static and dynamic power [1]. In generic terms, static power is the power consumed when the device is on but no signals are changing value while the dynamic power is consumed whenever the signal value changes [1].

In CMOS designs, the static power consumption is primarily due to leakage [3] whereas short circuit, glitching and switching power constitute dynamic power [3]. Till 180 nm technology node, dynamic power dominates the total power consumption [1]. However, at lower technology nodes, there is an increase in leakage power due to smaller feature size and threshold voltage reduction. As a result, leakage power surpasses dynamic power and becomes major contributor to total power of the design.

The short circuit power in CMOS designs is due to finite rise time and fall time of inputs, which makes both Pull Up Network (PUN) and Pull Down Network (PDN) simultaneously on. The finite propagation delay of gates may cause spurious transitions at the output and power dissipated in such an event is termed as glitching power [3]. Switching power is the power dissipated due to charging and discharging of capacitive loads. The switching power may be reduced by controlling physical capacitances, switching activity, clock frequency and supply voltage [3]. Some of the prevailing techniques to address these are clock gating [49-55], Multiple Supply Voltage (MSV) [56-65], Dynamic Voltage and Frequency Scaling (DVFS) [63-65] and Adaptive Voltage Scaling (AVS) [65-66].

The clock gating [49-55] minimises dynamic power by controlling the switching activity of the circuit. The basic idea behind the concept is to block the clock signal to the parts of circuit in which there is no change in value of output or to parts of circuit in which the stored value remains unchanged. To implement clock gating in a design, three cells have been used- gate based cell, latch-based cell, and flip flop-based cell [49-55]. The performance of these variants is compared in terms of power, area, and performance in [51]. It is inferred that for low power, gate-based cell is used while latch-based cell is suitable for high performance. Flip flop-based cell compromises both power and performance. In gate-based cell, glitching problem exists while latch-based cell suffers from sleep period i.e., a change in enable signal is not captured during this time which may lead to faulty design. Different types of flip flop [53-55] have also been designed using clock gating technique to reduce dynamic power.

The MSV technique [56-65] is yet another method used for dynamic power reduction in CMOS circuits. This technique involves supplying different parts of the circuit with

different voltages to reduce power while maintaining performance [56-58]. The dual supply technique at gate level is used in [57,58] by assigning low supply voltage to gates and flip flops lying on the critical path. There has been significant research in this area, including a new technique that combines critical/non-critical paths and switching activity analysis to assign different supply voltages [56]. In addition, energy efficient level converters have also been designed to overcome the delay and energy penalty associated with dual supply voltage designs [59-62]. A new low power level shifter is also presented for MSV designs in [60]. It uses multi-threshold CMOS technique and topological modifications to guarantee a wide voltage conversion range with limited penalty on static power and total energy consumption.

Another method of dynamic power reduction in CMOS is DVFS technique [63-65]. As dynamic power depends on voltage and frequency, so this dependence is used for DVFS technique [63,64]. Here, the voltage and frequency of the design are scaled dynamically for power reduction. It involves dynamically adjusting the supply voltage and clock frequency of a circuit based on its workload. Recent research has focused on developing novel DVFS techniques, such as per-core, per-chip, and cluster-level DVFS techniques [64], and AVS technique [65-66] to optimize power savings while maintaining performance. A separate voltage regulator is used for each core in per-core DVFS to have more control over power resulting in increased number of voltage regulators. This problem is resolved in per-chip DVFS by employing a single voltage regulator while compromising flexibility. So, to arrive at an intermediate solution, cluster level DVFS is proposed in [64]. In this technique, cores are grouped into multiple clusters depending on the workload and are driven by multiple regulators. The granularity of the design influences the efficiency and the cost of implementing DVFS. In AVS technique [65-66], voltage and frequency are dynamically

adjusted using a control loop. It achieves significant dynamic power reduction compared to open-loop voltage scaling techniques.

Another component which contributes significantly to total power is leakage power. In CMOS, it is caused by reverse bias diode leakage current, band-to-band tunnelling current, subthreshold leakage current, oxide tunnelling current hot carrier injection gate current, Gate Induced Drain Leakage (GIDL) current and channel punch through current [67]. Leakage power is now considered as the principal contributor to the total power consumption in many battery powered portable devices [67]. So, it necessitates the development of techniques to address leakage power issue. The first classification of leakage reduction techniques involves using different threshold voltage for transistors to minimize leakage [68-73]. Power gating is a technique that blocks current to unused parts of the circuit using sleep transistors [68]. Multi-threshold CMOS (MTCMOS) is another power gating technique that uses high threshold voltage transistors as sleep transistors to reduce leakage [68]. Dynamic Threshold MOSFET (DTMOS) involves varying the substrate bias with gate voltage to change the threshold voltage of a transistor dynamically [69-70], while Variable Threshold CMOS (VTCMOS) uses the concept of body effect to generate low and high threshold voltage for different transistors in the design [71]. The dual threshold technique assigns different threshold voltage to transistors based on the concept of critical and non-critical path [72]. VLSI CMOS LEAkage Reduction Technique (VCLEARIT) involves an additional circuit for sleep mode consisting of standard threshold voltage transistors and one high threshold voltage transistor to reduce leakage [73]. These techniques have certain drawbacks, such as additional sleep signal generation, increase in area and delay due to sleep transistors, and computational overhead of defining algorithms to decide the criticality of the paths involved.

Leakage reduction techniques can be further classified based on the concept of using stacking effect for leakage reduction [74-83]. Stacking effect states that leakage current reduces when the number of OFF transistors in the stack increases [74]. Techniques such as forced stack [74], sleepy stack [75], novel sleep technique [76], LEakage Control TransistOR (LECTOR) [77-79], GAted LEakage TransistOR (GALEOR) [80], GALEOR Stack [81], Leakage Control NMOS Transistor (LCNT) [82], Input-Controlled Leakage Restrainer Transistor (ICLRT) [83], Self-Control Leakage-Suppression Block (SCLSB) [84], Diode footed domino [85], LECTOR with footed diode [78], Lector based dual-Vt domino logic [79], Foot Driven Stack Transistor Domino Logic (FDSTDL) [86] and Domino Logic with Clock and Input Dependent Transistors (DOIND) [87] are based on this effect. Forced stacking technique uses two stacked transistors to reduce leakage current [74], while sleepy stack technique uses a high threshold voltage sleep transistor in parallel with the stacked transistors [75]. The novel sleep transistor technique connects a high threshold NMOS transistor in the PUN and a high threshold PMOS transistor in PDN [76]. The LECTOR technique inserts two Leakage Control Transistors (LCTs) between PUN and PDN to reduce leakage current [77], while GALEOR uses Gated Leakage Transistors (GLTs) [80]. Both the techniques use additional transistors to introduce stacking for leakage power reduction. However, both techniques suffer from limitations such as reduced output voltage swing, signal quality problems, and increased delay. The GALEOR Stack technique combines the GALEOR and forced stack technique, where half-size transistors are used along with high threshold GLTs between PUN and PDN [81]. This leads to a significant reduction in leakage power. The LCNT is another technique that uses two NMOS transistors between PUN and PDN [82]. It achieves better leakage power reduction with less delay penalty than LECTOR and GALEOR. However, it suffers from the disadvantage of having a low voltage level for

logic low signals. ICLRT-based method attaches an input-controlled PMOS and an NMOS ICLRT to each path leading from either the supply voltage or the ground to the output. SCLSB inserts two PMOS and two NMOS transistors between PDN and PUN to increase resistance and decrease leakage current [83]. All these techniques reduce leakage power, but some have an area or delay penalty, and some require additional hardware for sleep signal generation.

Various techniques have also been proposed to reduce leakage power in domino circuits [78-79,86-87]. These include using the LECTOR technique with footed diodes [78] and multi-threshold domino [79], using FDSTDL with transistor stacking [86], and introducing DOIND transistors with controlled gate terminals to reduce leakage current [87]. These techniques involve additional transistors and may incur delay and area penalties, and some require specific input selection or additional hardware.

The third category of leakage reduction techniques includes hybrid designs and miscellaneous techniques [88-92]. These techniques combine multiple concepts to reduce leakage power. Examples include drain gating technique which uses stacking and sleep transistors [88], a hybrid design that combines Trimode MTCMOS power and ground gated techniques [89], and a novel technique that combines gate-level body biasing and DTMOS [90]. Other techniques include INput DEPendent (INDEP) [91], which uses input-dependent transistors, and ON/OFf LogIC (ONOFIC) [92], which provides a high-resistance path between supply and ground. These techniques offer reduced leakage power and improved performance but may also have limitations such as the need for extra control or computational overhead.

### 1.2.2 State of the art- Alternative Logic Styles

A wide range of alternative logic styles exist in literature- PTL [8,93,94], GDI [9,10,95-97], DML [14-16,98-105], DMTGDI [17,18], DMPL [19,100] and DCVSL[11-13]. The PTL uses pass transistor network to implement different logics with less transistor count and delay [8], while GDI combines CMOS and PTL logic styles and suffers from output voltage swing problem and low drive capability [9]. Various modifications have been proposed to overcome these issues, including using Conventional Complementary Metal-Oxide Semiconductor (CCMOS) based inverters [95] and adding additional transistors for level restoration [96]. These modifications improve the performance of GDI with reduced power consumption, corrected swing degradation, and increased performance.

The DML is yet another logic style [15,98] that offers two operational modes - static and dynamic - for power reduction and high performance, respectively. The DML can be implemented using two topologies, type A and type B, and various techniques have been proposed for DML to minimize power consumption and area [99-105]. Mixed mode of operation [99,101], which combines static and dynamic modes, has been exploited for energy efficiency in DML-based carry save adders and multipliers [99]. Leakage reduction techniques, such as the self-controllable voltage level logic [100], have also been employed to reduce power in both static and dynamic modes. Additional controllers have been added to identify parts of the circuit to be operated in low power static mode and high-speed dynamic mode, which is referred to as mixed mode of operation [100]. Further a self-adaptive mechanism is used with DML logic style to operate the circuit in mixed DML mode [101]. A DML-based comparator has also been presented in [103] with high speed and low power

consumption by limiting the switching operations of internal nodes. However, some of these techniques have led to an increase in area overhead due to the presence of additional circuitry.

In addition to these, novel DML based logic styles are proposed which aims at exploiting DML benefits with minimum area or number of transistors. Two such logic styles are DMPL [19,102] and DMTGDI logic [17,18]. The DMPL design combines energy efficiency of PTL in static mode with high performance of DML design in dynamic mode [19]. A standard DMPL gate replaces the minimum size network of a DML design with a minimum-sized PTL-based network [19]. In [17], a modification to GDI logic, referred to as Transmission Gate Diffusion Input (TGDI), is introduced. Additional transistors are used in TGDI to provide dual mode operation and the design so arrived is called DMTGDI [17]. Various logic functions can be implemented with a few transistors using this logic style [17]. Both DMPL and DMTGDI configurations suffer from contention issue in dynamic mode of operation, so transistor sizing is critical to maintain proper voltage level at the output.

The DCVSL is another logic style that has been shown to be energy efficient and can exist in static [11] and dynamic (clocked) [12] configuration while providing output in true and complemented forms. This logic style utilizes NMOS logic trees to implement logic, which contributes to its high performance. While static DCVSL provides the advantage of reduced parasitic capacitance, it comes with increased power and complexity [11]. To improve performance, dynamic DCVSL designs have also been examined [12]. Leakage control technique has also been employed in both the static and dynamic configurations of DCVSL [11]. It involves the use of leakage control transistors and multi-threshold logic to achieve leakage reduction [11].

### 1.2.3 State of the art- Improved Transistor Technology

Research has also been done to search improved transistor technology with low power, high performance, and better control of device parameters. Improved transistor technology devices have allowed for successful implementation of many logic styles previously used in CMOS. Few of the technologies are- FDSOI [20-25,104,105], FinFET [27-35,106-110], CNTFET [36-48,111-118].

The FDSOI is an emerging technology that has several benefits compared to bulk silicon, such as a simplified manufacturing process and improved transistor performance [20-23]. By adding a thin layer of insulator beneath the channel, switching power is reduced, and channel control is improved. The Ultra-Thin Body and Buried Oxide FDSOI (UTBB FDSOI) utilizes an extremely thin transistor body that allows it to operate at lower voltage and with higher performance than conventional transistors [24,26]. The DML logic style, discussed earlier, has been successfully implemented using UTBB FDSOI technology, enabling the design of high energy efficient digital systems [99].

The FinFET, on the other hand, is another transistor technology, which can act as an alternative to CMOS as the devices are moving to lower technology node, allowing scaling of devices beyond 20nm [27-35,106-110]. Many of the logic styles- PTL, GDI, Transmission Gate Logic (TGL), Complementary Pass Transistor Logic (CPL)-which existed in CMOS domain, have been successfully implemented using FinFETs [106-110] and it was found that these logic styles achieve significant PDP reduction in FinFET domain. Studies have also been carried out to reduce leakage in FinFETs [27-35]. Several leakage reduction techniques such as ONOFIC [27,34], LECTOR [34], Drain Gating [35], LCNT [109] and INDEP [110], which were originally developed for CMOS, have been implemented using FinFETs. The

results have shown that these techniques effectively reduce leakage power in FinFETs. Some of the new techniques i.e., Leakage Controlling Pass Transistor (LCPT), Self-Controllable Voltage Level (SVL) are also introduced for FinFETs. In [106], a variant of LECTOR and LCNT leakage reduction technique is proposed which incorporates N-type and P-type LCPTs to introduce stacking which reduces leakage. Further, LCTs are added as sleep transistors for enhanced leakage reduction. Another novel approach introduced in [107] is Self-Controllable Voltage Level (SVL) technique and involves the use of three different types of SCVL circuits - Upper (USVL), Lower (LSVL), and Type 3 (a combination of the upper and lower SVL circuit designs). The SVL technique is designed to reduce leakage power by controlling the voltage levels during the standby mode.

Another device which has gained popularity in digital domain mainly for low power designs is CNTFET [36-48,111-118]. Various MOSFET based logic styles, which are already discussed, have successfully been implemented in CNTFET domain and it is found that these CNTFET based logic styles- C-CMOS, CPL, domino, TG-CNTFET, GDI- exhibit better PDP as compared to conventional MOS [39]. The GDI logic style is popular in the CNTFET domain due to its excellent performance in terms of power, delay, and PDP, but it has a drawback of reduced output voltage swing [111-113]. To address this issue, a Modified GDI (MGDI) logic style has been proposed [112]. When combined with CNTFETs, the MGDI logic style produces smaller, faster, and higher performance devices compared to CMOS designs [112]. TGDI logic style is also utilized in the CNTFET domain, and offers improvements in power, delay, and PDP over traditional GDI [114].

In addition, these devices provide a unique opportunity to control threshold voltage by changing the chiral indices or the diameter of CNT. As a result, these devices are widely

used for multi-valued logic implementation also, proposed in [46-47]. Another area of research that has emerged in CNTFET domain is leakage power. Limited study has been conducted on the implementation of techniques for reducing leakage in CNTFETs, using the methods previously developed for MOSFETs [115-121]. In [115], the efficiency of two methods is assessed for lowering CNTFET subthreshold leakage. For leakage reduction, a negative bias is applied to the n-type CNTFET's gate in the first method, and pull-down networks are stacked in CNTFET-based designs, referred to as stack forcing in the second method. In [116], leakage reduction techniques- sleep transistor, forced stack, data-retention sleep transistor and stacked sleep have been investigated in CNTFET domain. It is found that these techniques are adept at reducing leakage even in CNTFET domain. However, they impose an area penalty. Some novel techniques have also been proposed for leakage reduction in CNTFETs [119-121]. One such technique is proposed in [119-120] which uses the concept of dual chiral indices (multi-VTH) to reduce leakage in CNTFETs. Another method, presented in [121], reduces subthreshold leakage current and improves the noise margin by introducing a feedback structure that controls the transistor's threshold voltage. Although many methods have been developed to address leakage in CNTFETs, research in this area remains limited. Therefore, there is a need to investigate additional strategies for reducing leakage in the context of CNTFETs.

## 1.3 Research Gaps

As the technology is scaled down to deep nanometre regime, power mainly leakage power, in CMOS based designs is increasing at an exponential rate. Many techniques have already been proposed to tackle this issue, but these techniques have some limitations associated with them, as already discussed. Another point to be noted is that in deep

nanometre regime, dynamic power is no more a dominant component of power in CMOS devices. Even after extensive research, the issue of increased power still persists especially when technology node is continuously scaled down. So, there is a need to search for transistor technology and logic styles, which can act as a substitute to CMOS so as to have power efficient designs. These emerging logic styles and technology inherently offer the advantage of low power along with other merits as compared to CMOS. Power reduction techniques are also required for these alternative logic styles to have low power designs. Further the improved transistor technology mainly FinFET, CNTFET and alternative logic styles can be explored and further power reduction is possible in the designs based on these. These new technologies offer great opportunity for low power designs with enhanced performance. So, the research gaps can be summarized as:

- There is a need for search of alternative logic styles and improved transistor technologies that can act as low power alternatives to CMOS.
- Power reduction techniques-specially targeting leakage power-need to be explored for alternative logic styles.
- For improved transistor technologies, the power reduction strategies can further be explored for low power designs.

## 1.4 Research Objectives

Based on the literature review and the research gaps identified thereafter, the following objectives are set for the research work:

- To develop techniques for leakage power reduction in alternative logic styles.
- To formulate techniques that mitigate total power in alternative logic styles

- Development of leakage power reduction techniques in circuits based on improved transistor technology.
- To investigate total power reduction methods in improved transistor technology-based circuit designs.

In order to achieve the objectives, the following are the highlights of the work carried out:

i. Two designs are proposed for leakage power reduction in footed DML circuits referred to as GALEOR with Dual Mode Logic (GDML) and GALEOR with Dual Mode Logic with footed Diode (GDMLD). Also, LECTOR technique is proposed for footed DML circuits referred to as LDML, which leads to significant leakage power reduction in footed DML circuits.

ii. A modification of DMTGDI logic style, referred to as Modified DMTGDI (M-DMTGDI) design, is presented which provides PDP reduction and resolves the contention issue in existing DMTGDI design. Also, a modification to existing static DCVSL design is proposed and is referred to as Dual Mode DCVSL (DM-DCVSL) design. The proposed design provides both power saving and delay reduction.

iii. CNTFET based Modified DMTGDI design and CNTFET based DMTGDI design, referred to as C-MDMTGDI design and C-DMTGDI design, respectively are proposed which offer PDP reduction. The proposed C-MDMTGDI design overcomes the contention issue in C-DMTGDI design. Further leakage reduction techniques-LECTOR, GALEOR and LCNT are proposed for C-MDMTGDI design.

iv. CNTFET based DML (C-DML) design is proposed which offers PDP reduction in both static and dynamic mode.

## 1.5 Organization of the thesis

Following is the brief description of chapters:

**Chapter 1:**

This chapter gives a background and literature review of power reduction in standard CMOS designs, alternative logic styles and improved transistor technologies. It further states the objectives set for exploring novel alternative logic styles and their power reduction.

**Chapter 2:**

This chapter presents an elaborative description of various alternative logic styles- DML, DMTGDI and DCVSL. For each alternative logic style, the operation and analysis of 2-input NAND gate is discussed.

**Chapter 3:**

This chapter discusses three novel leakage reduction techniques for footed DML design- LDML, GDML, and GDMLD. Firstly, the operation of the proposed designs is elaborated and then the simulative investigation of circuits based on proposed designs is done with functional verification and performance comparison.

**Chapter 4:**

This chapter is devoted to two proposed DML based designs- M-DMTGDI and DM-DCVSL. First existing DMTGDI and DCVSL designs are discussed and then the proposed designs are put forward with their operation and simulation results. Each of the proposed design based circuit is functionally verified and then a performance comparison is done.

**Chapter 5:**

This chapter elaborates the implementation of footed DML and M-DMTGDI design in CNTFET domain. Further, leakage reduction techniques-LECTOR, GALEOR and LCNT are also proposed for C-MDMTGDI design. Extensive simulation of the proposed designs is done to check the proposed design's functionality and a performance comparison is drawn between the existing and proposed design.

**Chapter 6:**

This chapter summarizes the work presented in the thesis and the future scope of the work.

All throughout the thesis, the simulations for functional verification and performance comparison for MOSFET based designs are performed using Symica DE tool and for CNTFET based designs, HSPICE tool is used.

# Chapter 2

# Alternative Logic Styles: Basic Concepts

## 2.1 Introduction

This chapter provides an overview of various alternative logic styles, delving into their fundamentals and operational aspects. The alternative logic styles covered in this chapter include DML, DMTGDI and DCVSL.

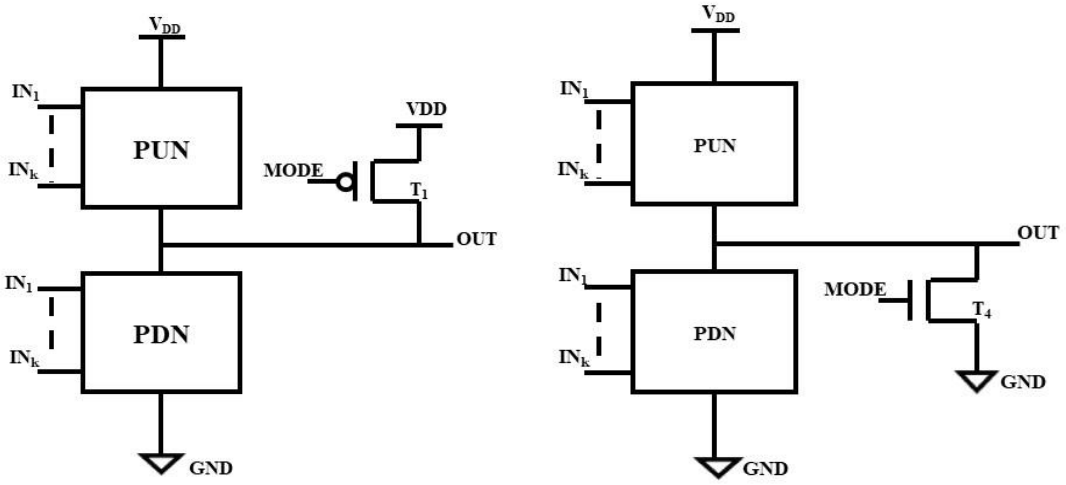
## 2.2 Dual Mode Logic (DML)

The DML is an alternative logic style which allows two operational modes in a design i.e., static and dynamic mode [14-16]. This logic family has two variants-unfooted and footed [14]. Further, two topologies i.e., type A and type B exist in each of these variants. The DML fundamentals and operation of DML 2-input NAND gate are discussed in the following subsections.

### 2.2.1 DML fundamentals

The unfooted DML design consists of PUN and PDN with an extra pre-charge/ pre-discharge transistor [15]. It can be implemented via two topologies- type A and type B as shown in Fig. 2.1. A pre-charge transistor ($T_1$) and pre-discharge transistor ($T_4$) is added at the output of a conventional CMOS gate for type A and type B topology respectively. In static mode, the MODE input is at logic “1” (logic “0”) for type A (type B) which makes transistor $T_1$ ($T_4$) off . For dynamic mode, a clock signal is used as MODE input which permits two phases of operation-pre-charge (pre-discharge) and evaluation for type A (type B). The output node is charged to supply voltage (discharged to ground (GND)) using $T_1$ ($T_4$) transistor in type A (type B) topology in pre-charge (pre-discharge) phase as MODE input is logic “0” (logic “1”). In evaluation phase of dynamic mode, the MODE input is logic “1” (logic “0”),

as a result, transistor $T_1$ ($T_4$) becomes off. The applied inputs decide the state of output in both type A and type B designs.




(a) (b)

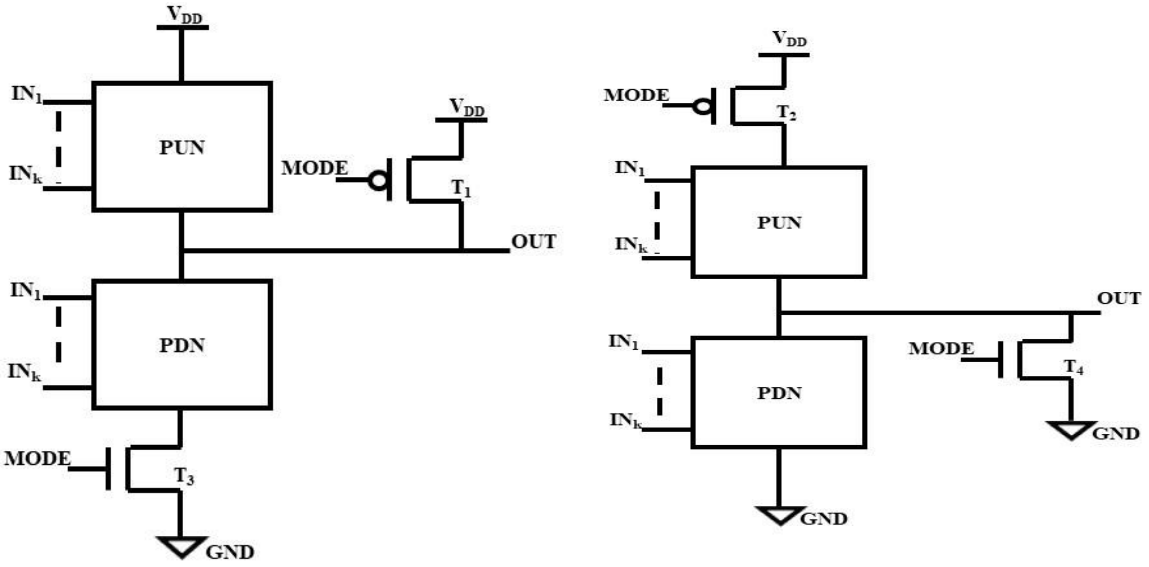
Fig. 2.1 DML design (a) Unfooted type A [14] (b) Unfooted type B [14]

Basic structure of a footed DML gate is given in Fig. 2.2. The type A footed design consists of an additional NMOS transistor ($T_3$), placed between PDN and ground along with pre-charge transistor ($T_1$), as shown in Fig. 2.2 (a). Similarly, for type B, this design includes an additional PMOS transistor ($T_2$) between PUN and supply voltage along with pre-discharge transistor ($T_4$), as shown in Fig. 2.2 (b). In static mode, the MODE input is at logic '1" for type A and logic "0" for type B topology [14]. The additional footer transistor ($T_3$) is turned on in type A. In type B topology, the header transistor ($T_2$) is turned on. For dynamic mode, a clock signal is used as MODE input which permits two phases of operation- pre-charge (pre-discharge) and evaluation for type A (type B).

For type A footed DML design, the output node is charged to $V_{DD}$ using $T_1$ transistor in pre-charge phase. At this time, the footer transistor ($T_3$) remains off. Analogously, the

output node is discharged to ground using $T_4$ transistor in type B footed DML topology in pre-discharge phase. The header transistor ($T_2$) remains off.

In evaluation phase, transistor $T_1$ is off for type A topology. At the same time, the additional footer transistor ($T_3$) is turned on. In type B topology, transistor $T_4$ is off and the header transistor ($T_2$) is on. As a result, the applied inputs decide the output in both type A and type B designs in evaluation phase.




(a) (b)

Fig. 2.2 DML design (a) Footed type A [14] (b) Footed type B [14]

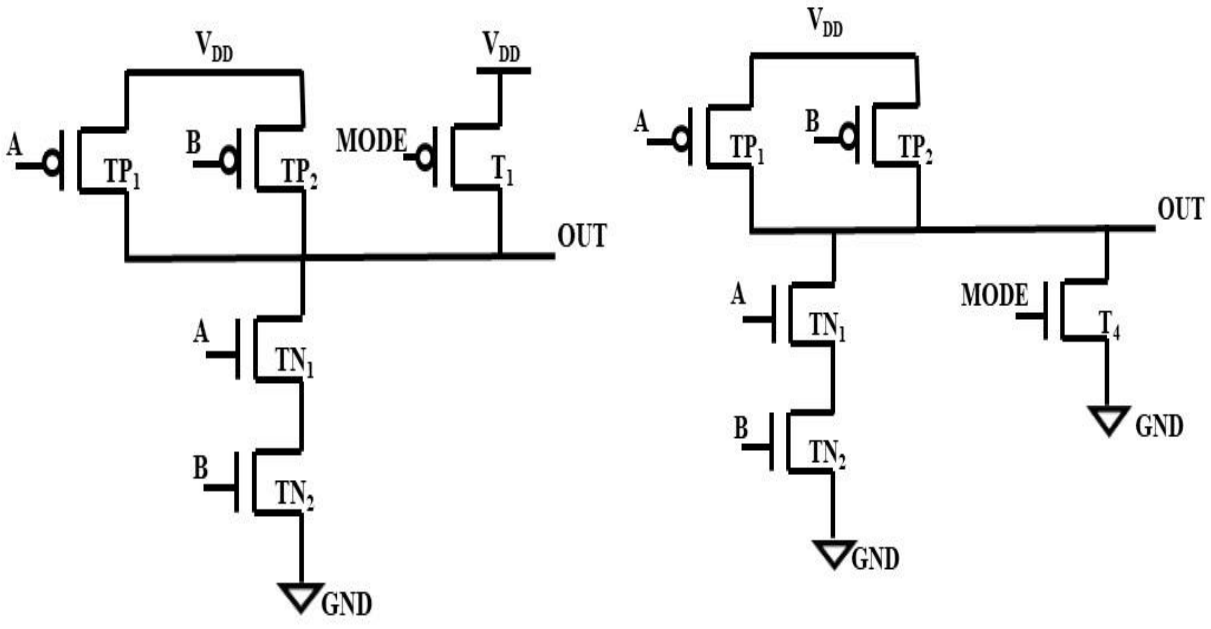
### 2.2.2 Operation of DML 2-input NAND gate

To understand the operation of both unfooted and footed DML design, a 2-input NAND gate is considered, as shown in Fig. 2.3 and Fig. 2.4. The operation of an unfooted DML based 2-input type A NAND gate is described next. In static mode, the MODE input is at logic "1" so the pre-charge transistor ($T_1$) remains off. The output is calculated according to the inputs applied. When (A, B) = (1, 1), both NMOS transistors $TN_1$,$TN_2$ are on, and

PMOS transistors $TP_1$,$TP_2$ are off. A direct path is created between output node and ground, resulting in logic “0” at the output. When the input (A, B) = (0, 0), both NMOS transistors $TN_1$,$TN_2$ are off and simultaneously, PMOS transistors $TP_1$,$TP_2$ are on. As a result, a path is created between output node and $V_{DD}$, causing a logic “1” at the output node. Similarly, in the case of (A, B)= (0, 1), the $TP_1$ and $TN_2$ transistors are on, while $TN_1$ and $TP_2$ transistors are off. Consequently, a connection forms between the output node and $V_{DD}$, leading to a logic “1” output. When (A, B)= (1, 0), the $TP_1$ and $TN_2$ transistors are off, while $TN_1$ and $TP_2$ transistors are on, thus creating a path between output node and $V_{DD}$ resulting in logic “1” output. Thus, the circuit realizes NAND function.

For dynamic mode, the MODE input is supplied with a clock signal having two phases of operation- pre-charge and evaluation. In pre-charge phase, as MODE input is logic “0”, transistor $T_1$ is on. Therefore, the output is charged to $V_{DD}$. In evaluation phase, MODE input is logic “1” so the pre-charge transistor ($T_1$) remains off. For inputs (A, B) = (1, 1), NMOS transistors $TN_1$,$TN_2$ are on, and PMOS transistors $TP_1$,$TP_2$ are off, causing a path to be created between output and ground. As a result, the output attains logic “0” value. When (A, B) = (0, 0), NMOS transistors $TN_1$,$TN_2$ are off, and PMOS transistors $TP_1$,$TP_2$ are on, thus creating a path between output and $V_{DD}$, which yields a logic “1” output. Similarly, with (A, B) = (0, 1), $TP_1$ and $TN_2$ transistors are on, while $TN_1$ and $TP_2$ transistors are off, creating output to $V_{DD}$ path to make output as logic “1”. Lastly, for (A, B) = (1, 0), $TP_1$ and $TN_2$ transistors are off, while $TN_1$ and $TP_2$ transistors are on. This establishes a connection between the output and $V_{DD}$, resulting in a logic “1” output.

Similar analysis can be done for unfooted DML based 2-input type B NAND gate in static and dynamic mode, as depicted in Fig. 2.3 (b). In static mode, the pre-discharge transistor ($T_4$) is off and the output is evaluated according to applied inputs. In pre-discharge phase of dynamic mode, pre-discharge transistor ($T_4$) is on and it discharges the output node to ground. In evaluation phase, the output is evaluated according to applied inputs, as the pre-discharge transistor ($T_4$) is off.



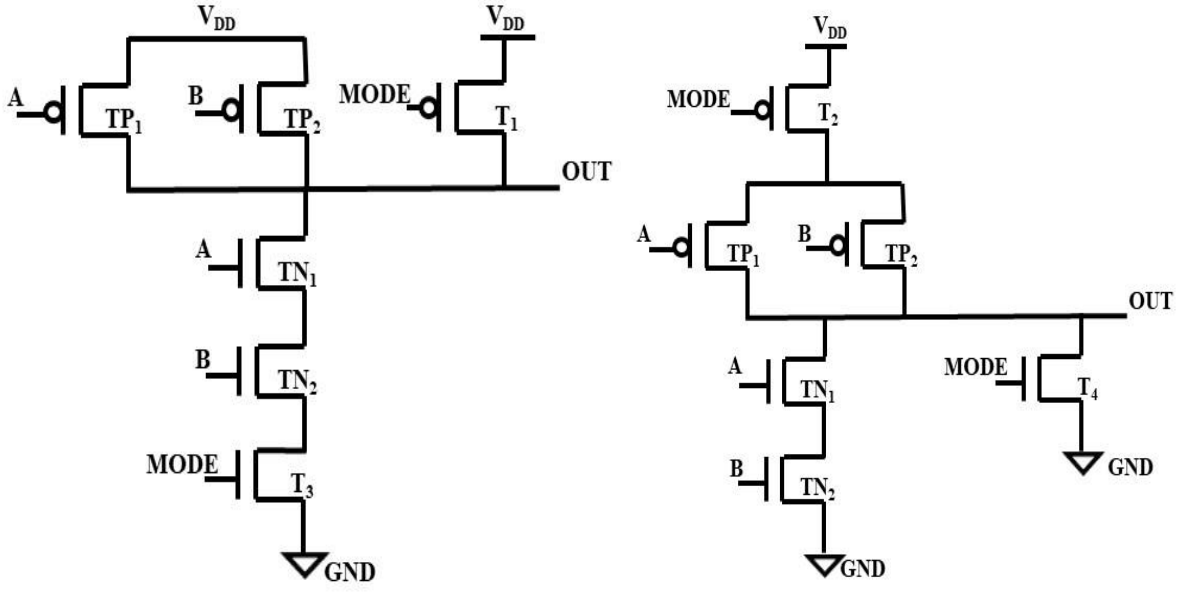

(a) (b)

Fig. 2.3 DML based 2-input NAND gate (a) Unfooted type A (b) Unfooted type B

Consider a footed DML based 2-input type A NAND gate, shown in Fig. 2.4 (a). In static mode, the operation is same as that of an unfooted DML based 2-input type A NAND gate with the pre-charge transistor $T_1$ as off and the footer transistor $T_3$ as on. For dynamic mode, the MODE input is supplied with a clock signal having two phases of operation- pre-charge and evaluation. In pre-charge phase, as MODE is logic "0", transistor $T_1$ is on,

footer transistor $T_3$ is off. Therefore, the output is charged to $V_{DD}$. In evaluation phase, the pre-charge transistor $T_1$ remains in the off state, while the footer transistor $T_3$ is turned on. The operation is same as that of an unfooted DML based 2-input type A NAND gate in evaluation phase.

Similar analysis can be done for footed DML based 2-input type B NAND gate in static and dynamic mode, as depicted in Fig. 2.4 (b). In static mode, the pre-discharge transistor ($T_4$) remains off, while the header transistor ($T_2$) is on, allowing the output to be assessed based on the inputs applied. In the pre-charge phase of dynamic operation, the header transistor ($T_2$) is off, and the pre-discharge transistor ($T_4$) is on to discharge the output node to ground. During the evaluation phase, the output is determined based on the applied inputs, with the pre-discharge transistor ($T_4$) turned off and the header transistor ($T_2$) as on.




(a) (b)

Fig. 2.4 DML based 2-input NAND gate (a) Footed type A (b) Footed type B

In unfooted DML design, specific input combinations can potentially lead to contention during the pre-charge phase because a path exists between the supply voltage and ground. Consequently, appropriate transistor sizing becomes necessary to guarantee a complete voltage swing at the output. To elucidate this, consider an unfooted DML based 2-input type A NAND gate in pre-charge phase with both inputs (A, B)= (1,1). In pre-charge phase, MODE is at logic "0" and the transistor $T_1$ starts charging the output node, OUT to $V_{DD}$. The PDN of NAND gate is on and it starts discharging the output node. Therefore, proper output voltage is not obtained in that case. Similarly, contention occurs in unfooted DML based 2-input type B NAND gate between the pre-discharge transistor ($T_4$) and PUN in pre-discharge phase when both inputs (A, B)= (0,0). This issue is resolved in footed DML gates due to the presence of footer and header transistor in type A and type B topology respectively. In a type A design, the discharging of the output is prevented by the off footer transistor ($T_3$) during the pre-charge phase. Similarly, in a type B design, the charging of the output node is prevented by the on header transistor ($T_2$) during the pre-discharge phase. Therefore, full output voltage swing is achieved. Additionally, the unfooted DML gates exhibit short-circuit power issues during the pre-charge phase, an extended pre-charge duration, increased sensitivity to process variation, and reduced overall robustness [15].

## 2.3 Dual Mode Transmission Gate Diffusion Input (DMTGDI)

The DMTGDI design introduces dual mode capability in TGDI design by incorporating an additional transistor (pre-charge/pre-discharge transistor) between the output node and the supply voltage/ground [17]. Similar to DML, this variant also supports both static and dynamic operating modes which can be selected using a mode signal [17-18].

It can exist in two topologies- type A and type B. The DMTGDI fundamentals and operation of DMTGDI 2-input NAND gate are discussed in the following subsections.

### 2.3.1 DMTGDI fundamentals

A typical DMTGDI cell is shown in Fig. 2.5. It has two topologies, type A and type B, similar to DML. It uses TGDI block and its internal structure is depicted in Fig 2.5 (a). To attain two operating modes i.e., static and dynamic mode, additional pre-charge transistor $T_1$ is employed for type A topology (Fig. 2.5 (b)) while an additional pre-discharge transistor $T_4$ is used for type B topology (Fig. 2.5 (c)). To operate the DMTGDI cell in static mode, the transistor $T_1$ ($T_4$) is turned off by applying a constant logic "1" (constant logic "0") as MODE input for type A (type B) topology. The output of the DMTGDI cell is evaluated according to the types of inputs applied to $I_0$, $I_1$ and select line, S. For dynamic mode, a clock signal is applied as MODE input, which allows two phases of operation- pre-charge/ pre-discharge and evaluation [17]. For type A design, in pre-charge phase, transistor $T_1$ is on as MODE is logic "0" and it pre-charges the output node to $V_{DD}$ while in evaluation phase, transistor $T_1$ is off and the output is evaluated according to the logic function implemented by the TGDI structure (transistors $TP_1$, $TN_2$, $TN_1$ and $TP_2$) of the DMTGDI cell [17-18]. For type B design in pre-discharge phase, transistor $T_4$ is on as MODE is logic "1", which discharges the output node to ground. In evaluation phase, as the MODE input is logic "0", transistor $T_4$ is off and the output is calculated according to the implemented logic function depending on the inputs applied. As the core of the DMTGDI cell remains the TGDI cell, it retains the versatility of TGDI cell and can be used to get various logic functions listed in Table 2.1.

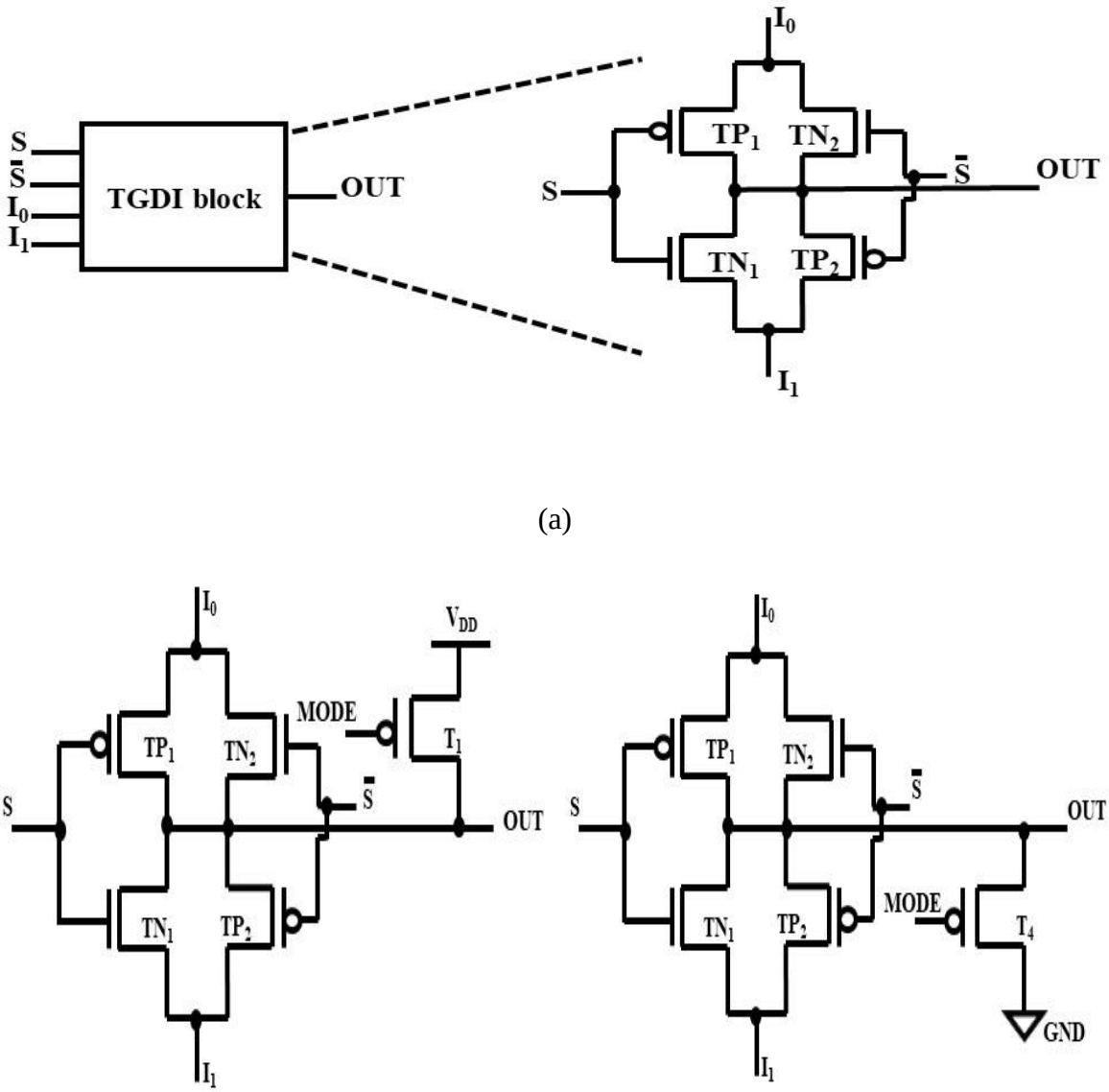



Fig. 2.5 (a) TGDI block and its internal structure (b) Type A DMTGDI cell [17] (c) Type B DMTGDI cell [17]

Table 2.1 Summary of logic functions realized by DMTGDI cell [17]

| $I_1$ | $I_0$ | S | $\bar{S}$ | LOGIC | FUNCTION |
|---|---|---|---|---|---|
| B | 0 | A | $\bar{A}$ | AB | AND |
| $\bar{B}$ | $V_{DD}$ | A | $\bar{A}$ | $\overline{AB}$ | NAND |
| 1 | B | A | $\bar{A}$ | A+B | OR |
| 0 | $\bar{B}$ | A | $\bar{A}$ | $\overline{A+B}$ | NOR |
| $\bar{B}$ | B | A | $\bar{A}$ | A⊕B | XOR |
| B | $\bar{B}$ | A | $\bar{A}$ | $\overline{A \oplus B}$ | XNOR |
| C | B | A | $\bar{A}$ | $\bar{A}$B+AC | MUX |

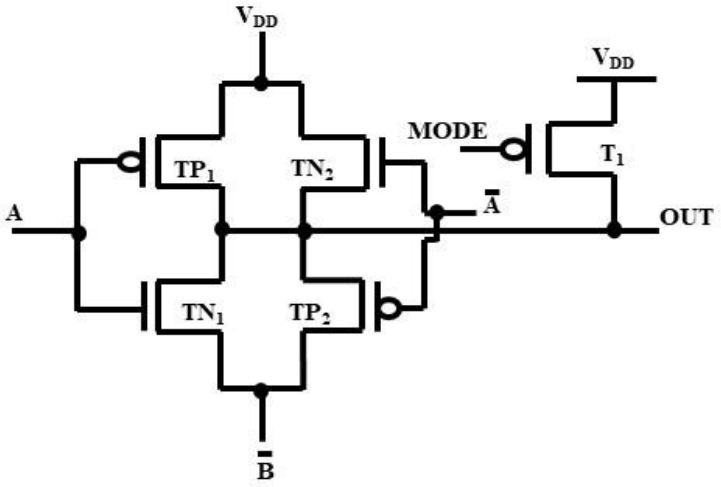
### 2.3.2 Operation of DMTGDI 2-input NAND gate

Consider a DMTGDI 2-input type A NAND gate (Fig. 2.6 (a)). The 2-input NAND function with A and B as inputs is described by (2.1).

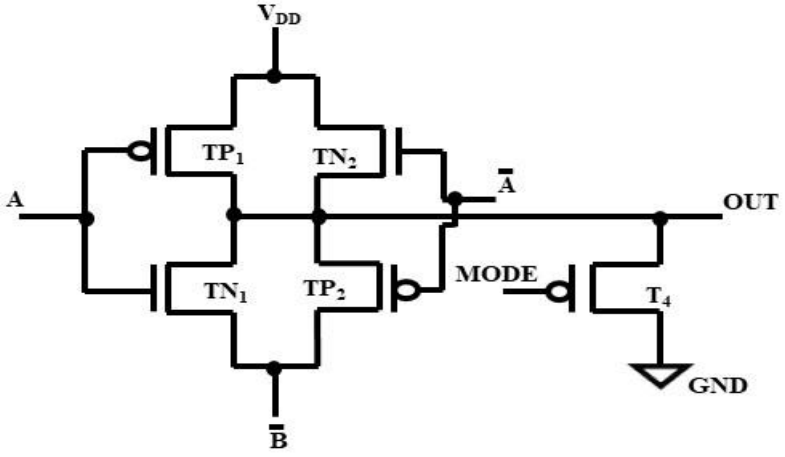
$$OUT = \bar{A}.\ V_{DD} + A.\ \bar{B} \quad (2.1)$$

In static mode, the MODE input is constant logic “1”. Therefore, transistor $T_1$ is off and the output of the gate depends on applied inputs. In the scenario where (A, B) = (1, 1), both $TP_1$ and $TN_2$ transistors remain off, and correspondingly, $TN_1$ and $TP_2$ transistors are also off. This leads to the output as logic “0”. When the input (A, B) = (0, 0), both $TP_1$ and $TN_2$ transistors are on, and simultaneously, the $TN_1$ and $TP_2$ transistors are on. This results in the creation of a path between output and $V_{DD}$ resulting in logic “1” value at the output. Similarly, in the case of (A, B)=(0, 1), the $TP_1$ and $TN_2$ transistors are on, while $TN_1$ and $TP_2$ transistors are on. Consequently, the output node gets connected to $V_{DD}$, resulting in logic “1” output. Lastly, when (A, B)= (1, 0), the $TP_1$, $TN_2$, $TN_1$ and $TP_2$ transistors are off. This establishes a path between output node and $V_{DD}$ which results in logic “1” output.

In dynamic mode, the MODE input is applied with a clock signal having two phases- pre-charge and evaluation. During pre-charge phase, MODE input is logic “0. Therefore, output node is charged to $V_{DD}$ irrespective of the applied inputs. In evaluation phase, the MODE input is logic “1” which makes transistor $T_1$ off. The output is evaluated according to the inputs applied and the analysis is same as in static mode for different input combinations.




(a)




(b)

Fig. 2.6 DMTGDI based 2-input NAND gate (a) Type A (b) Type B [17]

The DMTGDI based 2-input type B NAND gate is shown in Fig. 2.6 (b) and the analysis is same as that of DMTGDI based type A NAND gate. The only difference is that here, in static mode, the MODE input is constant logic “0. Therefore, transistor $T_4$ is off. In dynamic mode, for pre-discharge phase, MODE input is logic “1” which makes transistor $T_4$ on. The output is discharged to ground. For evaluation phase, the MODE input is logic “0, which makes transistor $T_4$ off. The output is evaluated according to the inputs applied to NAND gate.

In the DMTGDI design, certain input combinations can lead to contention during the pre-charge phase due to the presence of a path between the supply voltage and ground. Therefore, proper sizing of transistors is required to ensure full voltage swing at the output.

## 2.4 Differential Cascode Voltage Switch Logic (DCVSL)

Till now, the discussion has focussed on single ended alternative logic styles, specifically DML and DMTGDI. Now the discourse is extended to differential output alternative logic style i.e., DCVSL.

The DCVSL is a differential logic style that is derived from conventional CMOS logic and ratioed pseudo NMOS logic [11]. This design merges the strengths of these two traditional approaches, resulting in a high-speed and rail-to-rail logic style. It comes in both static [11] and dynamic configurations [12]. This logic style produces both differential outputs, the output and its complement. As a result, an extra inverter is not required to generate the complement of the output signal. Parasitic capacitance at the output nodes is reduced due to the exclusive use of NMOS transistors in PDN for implementing the logic function. This reduction results in a faster response time. To eliminate static power, two cross-connected PMOS transistors are used to provide positive feedback, ensuring that the

PUN and PDN are never on at the same time. When implementing complex logic functions, DCVSL enables the common transistors in the logic network to be shared for both differential outputs. While the static DCVSL reduces parasitic capacitance, it comes at the expense of increased power and complexity [11]. To enhance performance, a dynamic DCVSL design with both pre-charge and evaluation phases is employed [12]. The DCVSL fundamentals and operation of DCVSL 2-input NAND gate are discussed in the following subsections.

### 2.4.1 DCVSL fundamentals

A generic differential structure of static DCVSL [11] is illustrated in Fig. 2.7 (a), which is built using PDNs (PDN1 and PDN2) that exclusively uses NMOS transistors to implement a logic function (OUT) and its complement ($\overline{OUT}$). Two connected PMOS transistors ($TP_1$ and $TP_2$) are used to implement the PUN which form a positive feedback latch. Initially, assuming that OUT is logic "1" and $\overline{OUT}$ to logic "0", when the inputs are activated, both PDN1 and PDN2 evaluates. If the input combination applied causes PDN1 to turn on and create a discharge path for OUT, a conflict arises because $\overline{OUT}$, initially at logic "0", makes transistor $TP_1$ on. This results in a contention between transistor $TP_1$ and PDN1, preventing OUT from fully discharging at this stage. However, OUT begins to discharge slowly. Once OUT falls below the threshold voltage, transistor $TP_2$ is triggered to turn on, driven by OUT. Transistor $TP_2$ then provides a charging path for $\overline{OUT}$. Because PDN1 and PDN2 are mutually exclusive and implement differential logic functions, PDN2 remains off, and there is no discharge path for $\overline{OUT}$. Consequently, transistor $TP_2$ successfully charges $\overline{OUT}$ to $V_{DD}$. As $\overline{OUT}$ exceeds threshold voltage, transistor $TP_1$ turns off, interrupting the path between $V_{DD}$ and ground, thus eliminating any static power dissipation. Now PDN1 discharges OUT. Eventually, both OUT and $\overline{OUT}$ achieve the correct logic state.

Fig. 2.7 (b) shows a generalised structure of dynamic DCVSL [12]. It comprises two PDNs utilizing NMOS transistors to realize both the output (OUT) and its complement ($\overline{OUT}$). The clock (CLK) signal is used to control the working of the circuit. The dynamic DCVSL design works in pre-charge and evaluation phase when CLK is logic "0" and logic "1", respectively. During the pre-charge phase, transistors $TP_3$ and $TP_4$ are on, while transistors $TP_3$ and $TP_4$ are off, causing both output nodes to be pre-charged to $V_{DD}$. Any input change during this phase will not influence the output as there is no available path for current to flow from the output nodes to the ground. When a logic "1" CLK signal is applied, transistors $TP_3$ and $TP_4$ are turned off. Depending on the input values, one of the output nodes assumes a logic "0". The proper operation of the logic gate is ensured through the application of positive feedback to the PMOS pull-up transistors ($TP_1$,$TP_2$). To enhance the performance of the dynamic DCVSL gate, additional acceleration circuitry ($TN_1$,$TN_2$) is employed. This modification eliminates the contention that occurred during switching in the case of the static DCVSL gate. In static DCVSL, one of the PMOS transistors' (either $TP_1$ or $TP_2$) gates is logic "1" while the other is logic "0" since they are connected to complementary output nodes. Referring to Fig. 2.7 (a), consider a scenario where OUT needs to make a transition from logic "1" to logic "0" signifying that $\overline{OUT}$ must change from logic "0" to logic "1". When the inputs are activated, PDN1 activates and attempts to discharge OUT. However, this discharge process is hindered by $TP_1$, which remains on because $\overline{OUT}$ is at logic "0". This leads to a state of contention and static power is dissipated during this period. Now, the same scenario is analysed in dynamic DCVSL. Both OUT and $\overline{OUT}$ are pre-charged to $V_{DD}$ during the pre-charge phase of dynamic DCVSL. This infers that initially, both $TP_1$ and $TP_2$ are off.

This resolves the contention issue in dynamic DCVSL design since neither transistor $TP_1$ nor $TP_2$ is on initially.

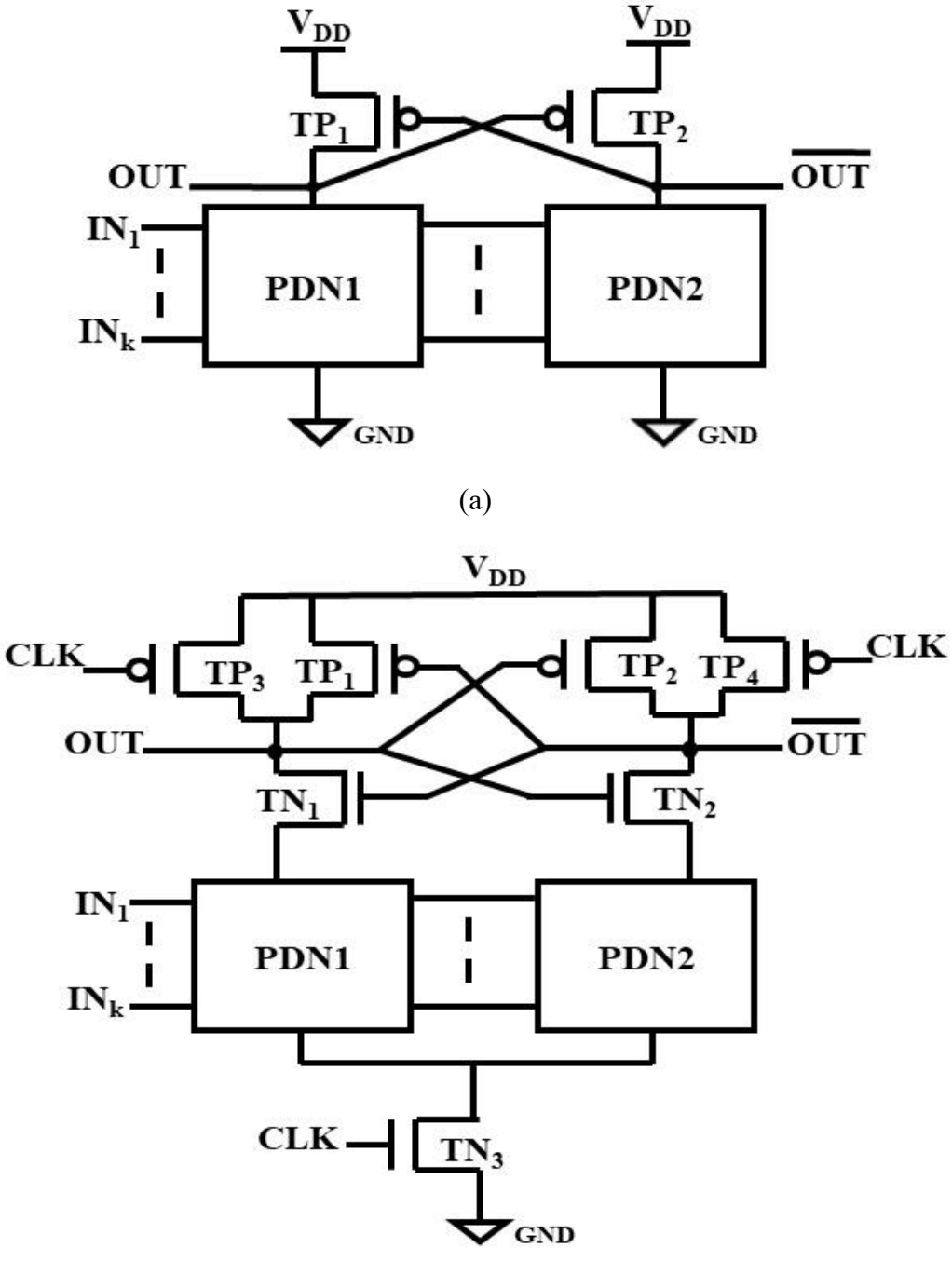


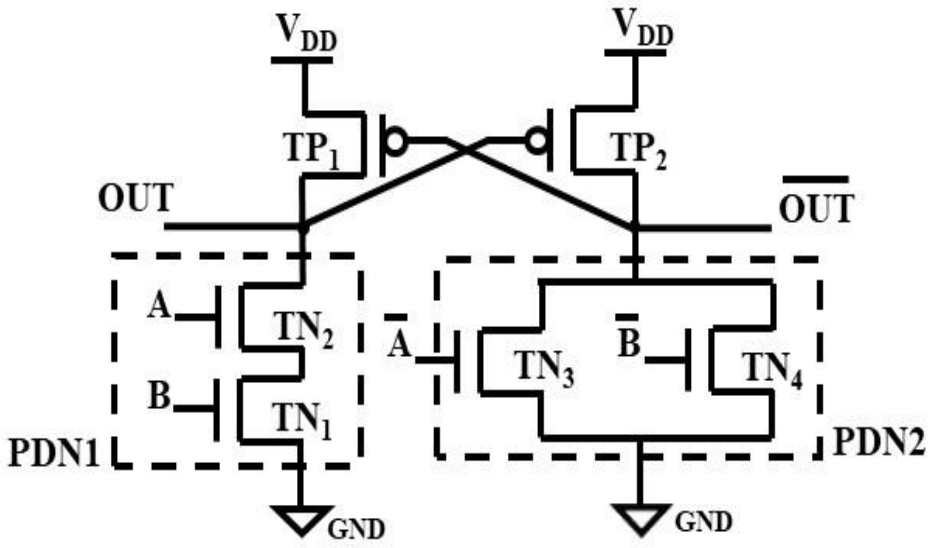

Fig. 2.7 DCVSL design (a) Static [11] (b) Dynamic [12]

### 2.4.2 Operation of DCVSL 2-input NAND/AND gate

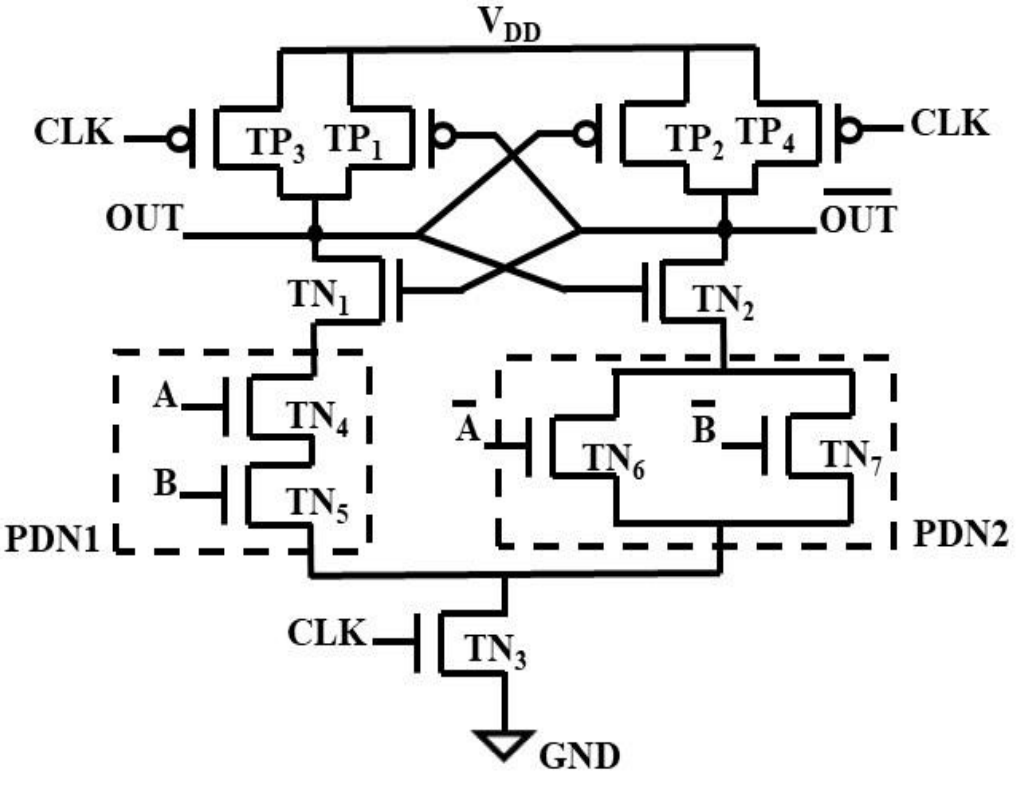
A static DCVSL NAND/AND consists of two stacked NMOS transistors implementing NAND logic and two parallel NMOS transistors driven by complementary inputs implementing differential AND logic. To illustrate the working, consider a static DCVSL based 2-input NAND/AND gate [11] shown in Fig. 2.8 (a), which consists of inputs- A, $\overline{A}$ , B and $\overline{B}$ and complementary outputs- OUT (NAND) and $\overline{OUT}$ (AND). Both PDN1 and PDN2 evaluate the logic function and its complement when the inputs are applied.

Initially, assuming that OUT is logic "1" and $\overline{OUT}$ to logic "0". When both (A,B) are logic "1", PDN1 ($TN_1$,$TN_2$) is turned on and a path is created for the output, OUT to discharge to ground. The transistor $TP_2$ is turned on due to discharging of OUT node. The transistor $TP_1$ is on due to logic "0" at $\overline{OUT}$. As a result, there is a contention between transistor $TP_1$ and PDN1, due to which there is a slow discharging of OUT. The complementary output, $\overline{OUT}$ is charged to $V_{DD}$ through transistor $TP_2$. When both the inputs are logic "0", PDN1 ($TN_1$,$TN_2$) is OFF and PDN2 is on and a path is created for the complementary output, $\overline{OUT}$ to discharge to ground. The transistor $TP_1$ becomes on, due to which the output, OUT is charged to $V_{DD}$. Similar analysis can be done for other two input cases of 2-input NAND/AND gate. As the two PDNs do not conduct simultaneously, proper rail-to-rail swing is obtained at the outputs- OUT and $\overline{OUT}$.

In dynamic DCVSL 2-input NAND/AND gate as illustrated in Fig. 2.8 (b), transistors ($TP_1$,$TP_2$) and ($TP_3$,$TP_4$) are off and on in pre-charge phase respectively. Due to which, both the complementary outputs are pre-charged to logic "1". The outputs are independent of inputs in this phase. In evaluation phase, transistors ($TP_3$,$TP_4$) are off, transistor $TN_3$ is on and the output is evaluated according to the inputs applied.




(a)




(b)

Fig. 2.8 2-input AND/NAND gate (a) Static DCVSL [11] (b) Dynamic DCVSL [12]

## 2.5 Conclusion

In this chapter, the fundamentals and operational aspects of the existing alternative logic styles- DML, DMTGDI and DCVSL are presented. The fundamentals cover the basic structure of each of the alternative logic style along with its working. Further, a 2-input NAND gate is considered to analyse each of the logic style in detail.

# Chapter 3

# DML Design With Leakage Power Reduction

The contents of this chapter are published in:

[1] N. Yadav, N. Pandey, and D. Nand, **"Leakage reduction in dual mode logic through gated leakage transistors,"** Microprocess. Microsyst., vol. 84, no. 104269, pp. 1-12, 2021, doi: 10.1016/j.micpro.2021.104269. (SCI indexing, 3.503 IF)

[2] N. Yadav, N. Pandey, and D. Nand, **"LDML: A proposal to reduce leakage power in DML circuits,"** Wirel. Pers. Commun., vol. 129, no. 2, pp. 1009–1024, 2023, doi:10.1007/s11277-023-10170-4. (SCIE indexing, 2.2 IF)

## 3.1 Introduction

Leakage reduction techniques have been widely studied in the context of static and dynamic CMOS designs, as already discussed in chapter 1. Limited study has been conducted to reduce leakage power in DML design. Two leakage control techniques are mainly used to reduce power in DML [123-125]. First technique uses sleep transistors for leakage power reduction and is popularly known as power gating technique [123-124]. It requires additional overhead for sleep control signal generation and its routing. The second technique employs multi-threshold concept [125], which requires identification of transistors whose threshold voltage is to be modified. The LECTOR and GALEOR are the leakage reduction techniques that are self-controlled and does not require any external signals or transistor identification for threshold modification [77,80]. Both LECTOR and GALEOR use LCTs and GLTs respectively, between PUN and PDN to introduce stacking so as to reduce leakage [77,80].

This chapter presents incorporation of LECTOR and GALEOR leakage reduction techniques for footed DML design. The LECTOR incorporated DML design implemented with standard threshold voltage and high threshold voltage LCTs, are referred to as LDML and LDML-HIGH-VTH design, respectively. The GALEOR incorporated footed DML design is referred to as GALEOR with Dual Mode Logic (GDML). Further, GDML design is extended by including a footed diode transistor, the design so obtained is referred to as GALEOR with Dual Mode Logic with footed Diode (GDMLD). The additional transistors- LCTs and GLTs reduce the leakage current in footed DML design without any complexity and routing overhead.

## 3.2 Leakage power in footed DML design

Leakage power ($P_{leakage}$) is predominantly due to subthreshold leakage current [2], given by (3.1) [2].

$$P_{leakage} = I_{subthreshold} * V_{DD} \quad (3.1)$$

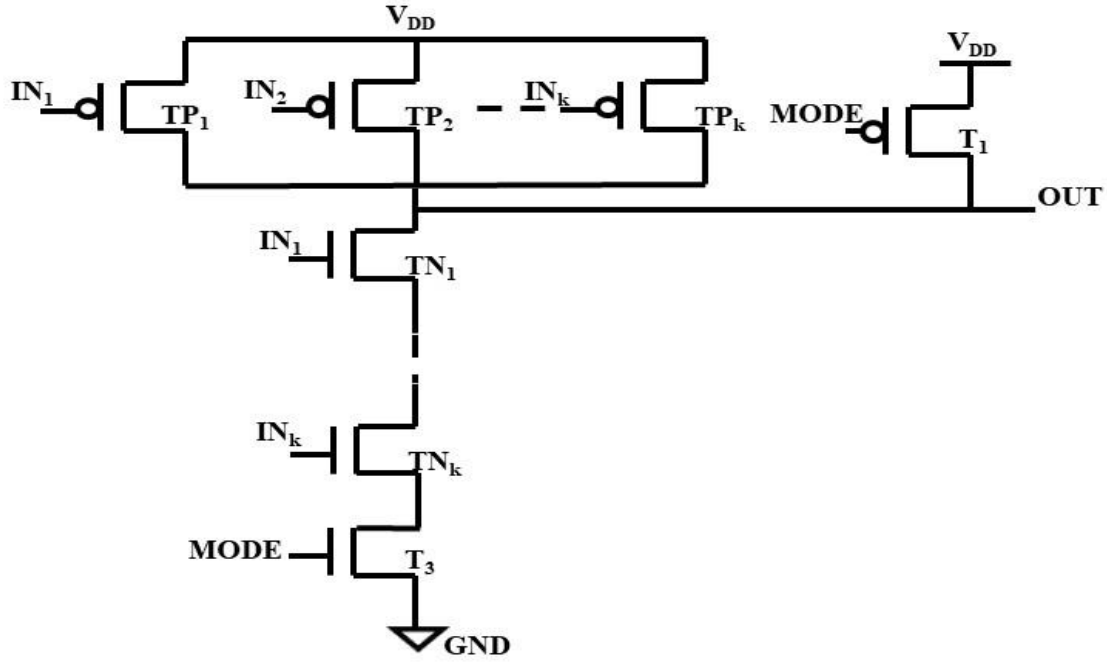
where $V_{DD}$ is supply voltage and $I_{subthreshold}$ is subthreshold leakage current given by (3.2) [2].

$$I_{subthreshold} = I_0 \exp ((V_{gs} – (VTH)/ \alpha V_t)) \quad (3.2)$$

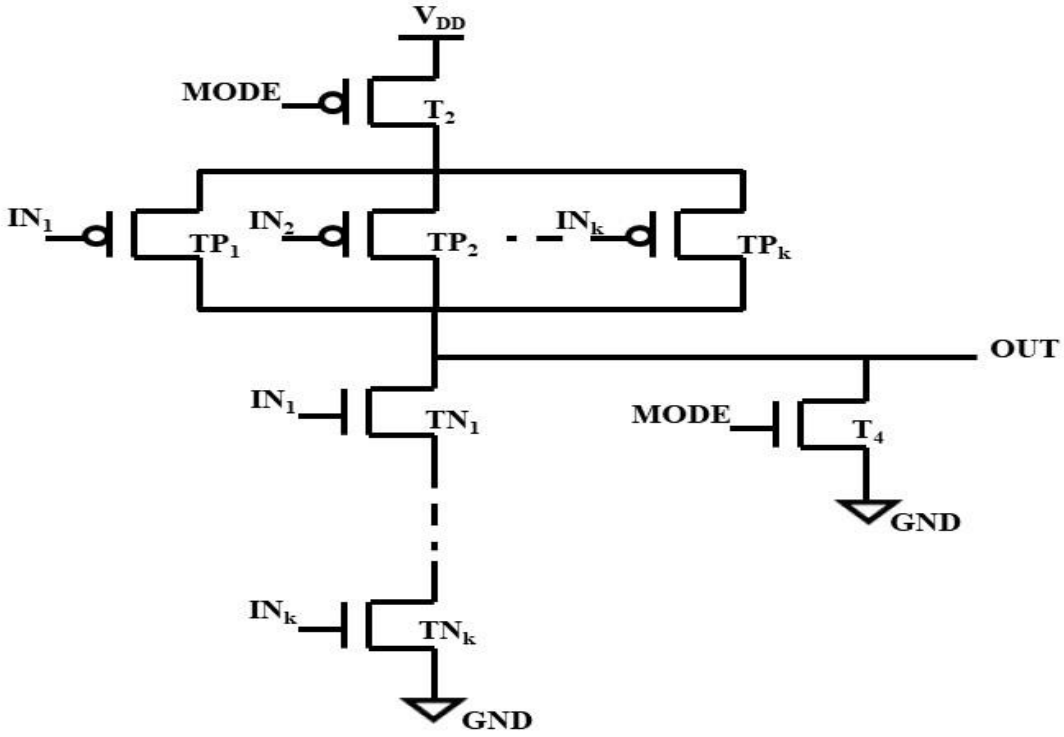
where VTH and $V_t$ correspond to the device threshold voltage and thermal voltage ($V_t$ = 25.9mV at room temperature); and $I_0$ is the current when Vgs = VTH. The parameter α is a constant depending on the device fabrication process, ranging from 1.0 to 2.5.

To investigate the presence of leakage current in footed DML designs, consider type A and type B footed DML NAND gate as shown in Fig. 3.1. In footed type A NAND gate, the pre-charge transistor $T_1$ remains off in static mode. Depending on the inputs applied, some amount of leakage current exists in the off transistors and in the off pre-charge transistor $T_1$. This creates a path for a current to flow from supply voltage to ground. Similarly, in pre-charge phase of dynamic mode, transistor $T_1$ is used to charge the output to supply voltage irrespective of the inputs applied. Ideally there should not be any current flowing in PDN as footer transistor $T_3$ is off but due to leakage in off transistors, leakage current flows from supply voltage to ground. During evaluation phase, the leakage current exists in off transistors and is dependent on the inputs applied. Similar analysis can be done for footed type B NAND gate in static and dynamic mode,

as depicted in Fig. 3.1 (b). The only difference is that in static and dynamic mode, additional leakage exists because of the pre-discharge transistor ($T_4$).




(a)




(b)

Fig. 3.1 Footed DML design (a) Type A NAND gate (TA-NAND) (b) Type B NAND gate (TB-NAND)

## 3.3 Proposed Design-I: LECTOR with DML logic (LDML)

The LECTOR was proposed as a technique to achieve leakage power reduction in various circuits by using the concept of stacking of transistors in the path from supply voltage to ground [77]. It is based on the concept that more leakage reduction is achieved if a greater number of off transistors are present in the path from supply voltage to ground [77]. In the proposed design-I (LDML), two LCTs are introduced between PUN and PDN of the footed DML design such that one of the LCTs is always near its cut-off region of operation. As a result, the effective resistance between supply voltage and ground is increased, which eventually reduces leakage.

### 3.3.1 Operation

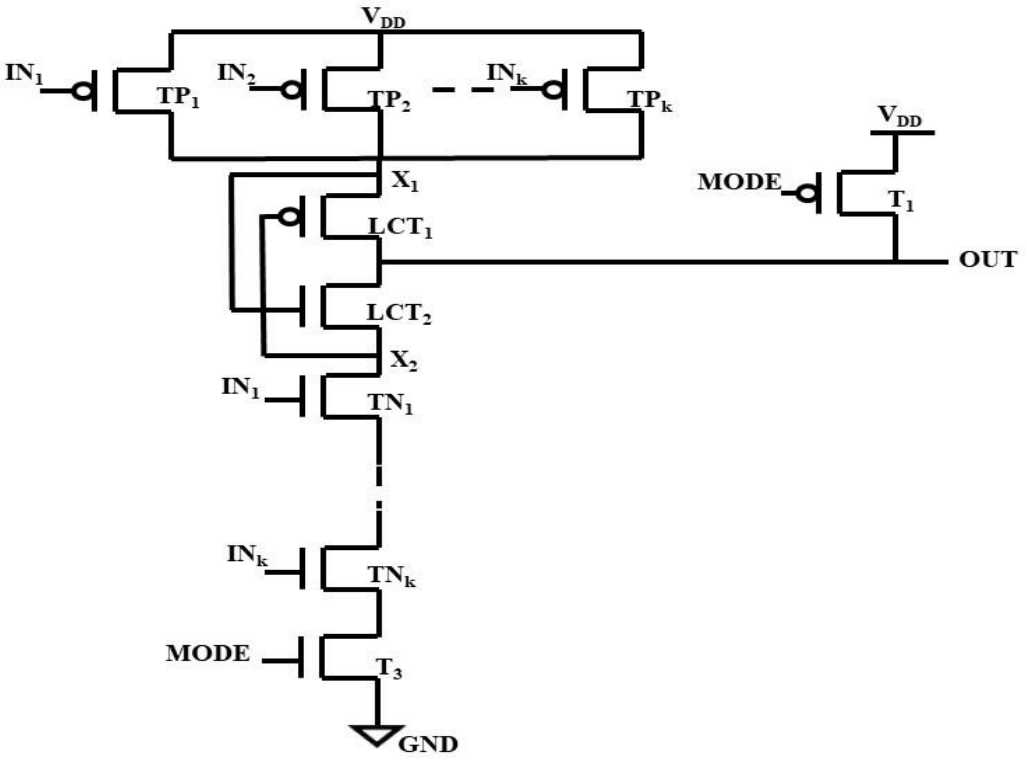
The proposed LDML design incorporates LCTs in footed DML design. Figure 3.2 depicts the proposed LDML Type A NAND gate (LDML-TA-NAND) and LDML Type B NAND gate (LDML-TB-NAND). Here $LCT_1$ (PMOS) and $LCT_2$ (NMOS) are introduced in Type A (TA-NAND) and Type B NAND (TB-NAND) footed DML gate, as shown in Fig. 3.1. It may be noted that the gate of $LCT_1$ is connected to source of $LCT_2$ and vice-versa. The drain of both $LCT_1$ and $LCT_2$ are connected to the output node.

In static mode of proposed LDML type A NAND gate, the MODE input is constant logic “1”. Therefore, transistor $T_1$ is off while transistor $T_3$ is on. The output of the gate depends on applied inputs. If all inputs are logic “1”, then transistors $TN_1$-$TN_k$ are on and $TP_1$-$TP_k$ remain off. Transistor $LCT_1$ is on and $LCT_2$ is off. Therefore, the output attains logic “0” value. Due to presence of off $LCT_2$ transistor in the path from supply voltage to ground, the effective resistance increases along the path, which results in less leakage current. Further, when all inputs are set to logic “0”, transistors $TN_1$-$TN_k$ are off and $TP_1$-$TP_k$ remain on. Transistor $LCT_1$ is off and $LCT_2$ is on. Therefore, the

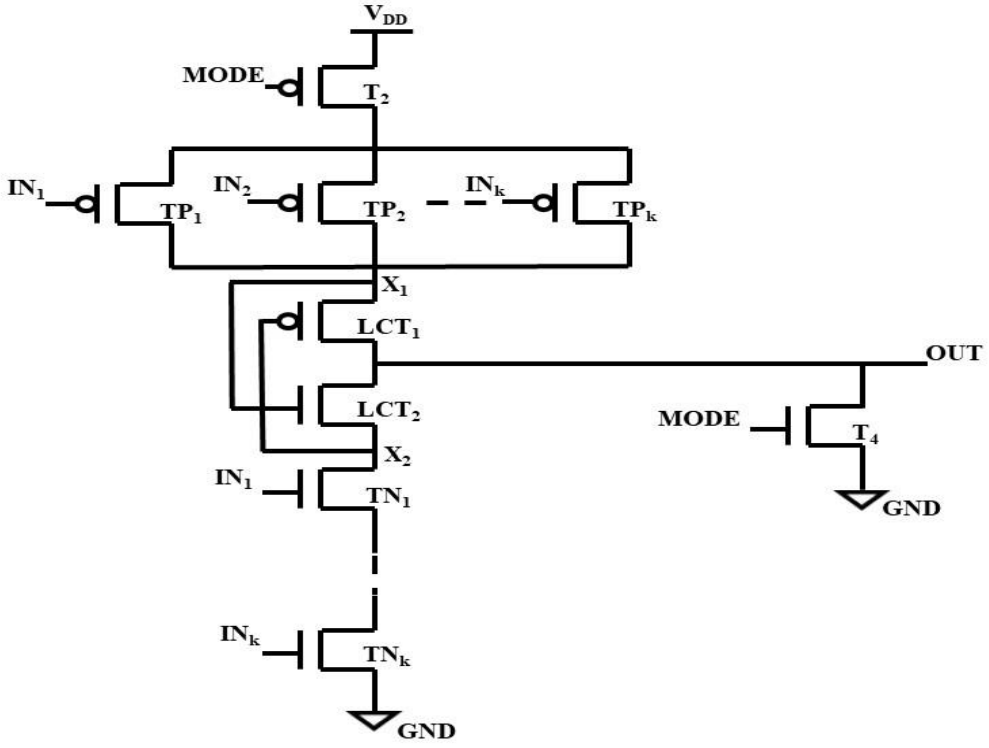
output attains logic “1” value. Due to presence of off $LCT_1$ transistor in supply voltage to ground path, the effective resistance increases, which results in less leakage current.

The operation of proposed LDML-TA-NAND gate in dynamic mode is elucidated here. The MODE input is applied with a clock signal having two phases- pre-charge and evaluation. During pre-charge phase, MODE input is logic “0”. Therefore, output node is charged to $V_{DD}$ irrespective of the applied inputs. However, the leakage current depends on the inputs applied. The status of LCTs is similar to that of static mode. The presence of LCTs increases the effective resistance from supply voltage to ground, leading to a reduction in leakage current.

In evaluation phase, the MODE input is logic “1” which makes transistor $T_1$ off and transistor $T_3$ is on. The output is evaluated according to the inputs applied. When all inputs are set to logic “1”, transistors $TN_1$-$TN_k$ are turned on while $TP_1$-$TP_k$ remain off. As a result, transistor $LCT_1$ is also turned on while $LCT_2$ remains off, causing the output to be at a logic “0” value. The presence of the off $LCT_2$ transistor in the path from the supply voltage to ground increases the effective resistance along the path, resulting in reduced leakage current. On the contrary, when all inputs are set to logic “0”, transistors $TN_1$-$TN_k$ are turned off while $TP_1$-$TP_k$ remain on. This causes transistor $LCT_1$ to be turned off while $LCT_2$ is turned on, resulting in the output attaining a logic “1” value. The presence of the off $LCT_1$ transistor in the path from the supply voltage to ground increases the effective resistance along the path, which in turn reduces the leakage current.




(a)




(b)

Fig. 3.2 Proposed LDML design (a) Type A NAND gate (LDML-TA-NAND) (b) Type B NAND gate (LDML-TB-NAND)

The proposed LDML type B NAND is shown in Fig. 3.2 (b) and the leakage mechanism is same as that of LDML type A NAND gate. The only difference is that here, in static mode, the MODE input is constant logic "0". Therefore, transistor $T_4$ is off while header transistor $T_2$ is on. In dynamic mode, for pre-discharge phase, MODE input is logic "1" which makes transistor $T_4$ on. The output is pre-discharged to ground. For evaluation phase, the MODE input is logic "0", which makes transistor $T_4$ off and transistor $T_2$ on and the output is evaluated based on inputs.

Further, in the proposed LDML-HIGH-VTH design, due to the presence of high VTH LCTs, the effective resistance of the path from supply voltage to ground is more than that of LDML design with standard VTH LCTs. As a result, the reduction in leakage current is more for LDML design with high VTH LCTs as compared to the standard VTH LCTs design.

### 3.3.2 Simulation results

This section is divided into two parts- the first subsection deals with the functional verification while the second subsection compares the performance of 2-input NAND gate, 2-input NOR gate and 1-bit FA based on proposed LDML and LDML-HIGH-VTH designs with corresponding footed DML counterparts. All the circuits are simulated using 90nm and 45nm BSIM4 model card for bulk CMOS with supply voltage of 1.2V and load capacitance of 5fF using Symica DE tool. Corner analysis is also done for 2-input NAND gate. Effect of voltage and temperature variation is also investigated. The SPICE simulator SymSpice is used to demonstrate the operation of proposed circuits and SymProbe tool is used for leakage power and delay analysis.

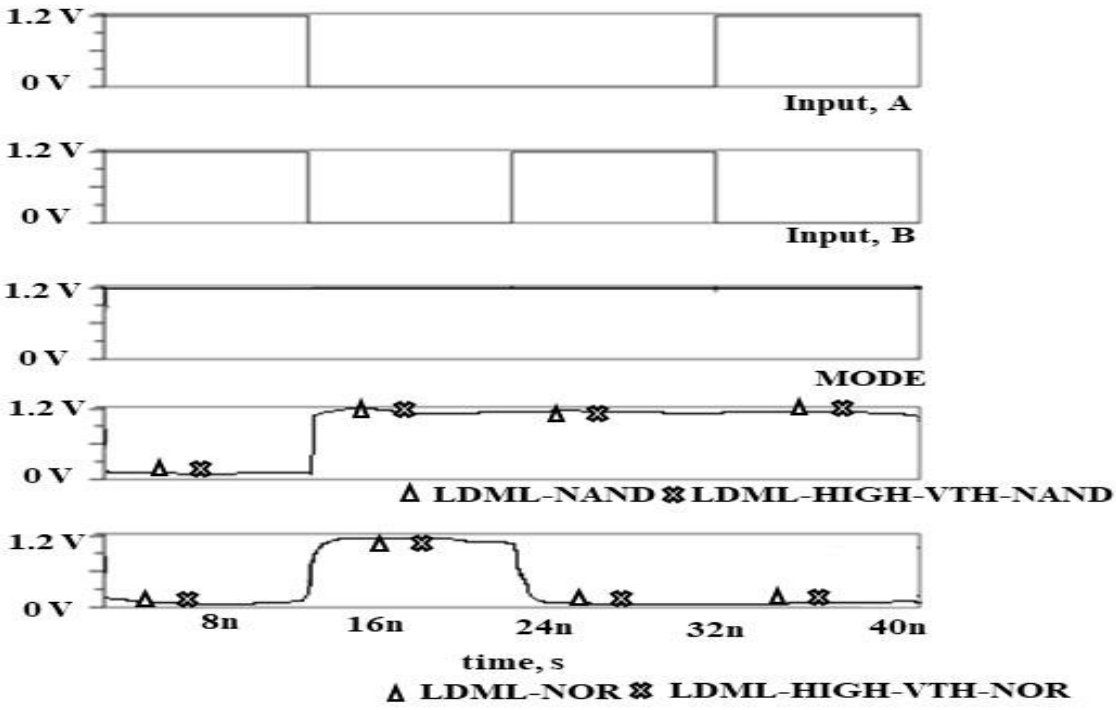
#### 3.3.2.1 Functional verification

The 2-input NAND and NOR circuits are implemented using the proposed LDML and LDML-HIGH-VTH design in type A and type B topologies. Figure 3.3 shows the

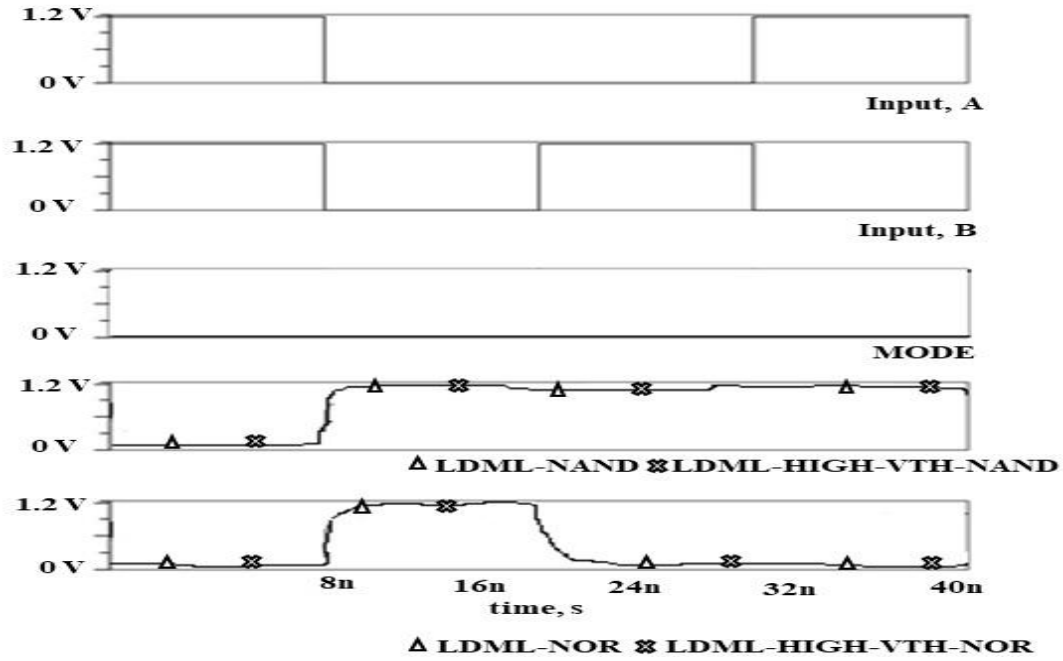
transient waveforms for 2-input LDML, LDML-HIGH-VTH type A and type B NAND (LDML-NAND,LDML-HIGH-VTH-NAND) and NOR (LDML-NOR,LDML-HIGH-VTH-NOR) gates in static mode. The MODE input is logic "1" for type A and logic "0" for type B in static mode. It may be noted that output for NAND gate is logic "1" when any of the inputs is logic "0" whereas NOR gate provides output logic "0" when any of the inputs is logic "1" for both type A and type B topology in static mode. Thus, both LDML and LDML-HIGH-VTH based NAND and NOR gate work correctly in static mode.

The dynamic mode of operation is depicted in Fig. 3.4. Here MODE input is connected to a clock signal having two phases of operation- pre-charge and evaluation. The transient waveforms for type A NAND and NOR gates in dynamic mode are illustrated in Fig. 3.4 (a). In pre-charge phase, MODE input is logic "0" for proposed type A gates so the output is charged to supply voltage for both NAND and NOR gates. Alternatively, in evaluation phase, the MODE is logic "1". The output for NAND gate is logic "1" when any of the inputs is logic "0" whereas NOR gate provides output logic "0" when any of the inputs is logic "1". Thus, both the type A NAND and NOR gates based on LDML and LDML-HIGH-VTH function correctly in dynamic mode.

The transient waveforms for type B NAND and NOR gates in dynamic mode are illustrated in Fig. 3.4 (b). In type B topology, the only difference is that for pre-discharge phase, the MODE input is logic "1" which discharges the output node and for evaluation phase, the MODE input is logic "0". The output for NAND gate is logic "1" when any of the inputs is logic "0" whereas NOR gate provides output logic "0" when any of the inputs is logic "1". Thus, both the type B NAND and NOR gates based on LDML and LDML-HIGH-VTH function correctly in dynamic mode.

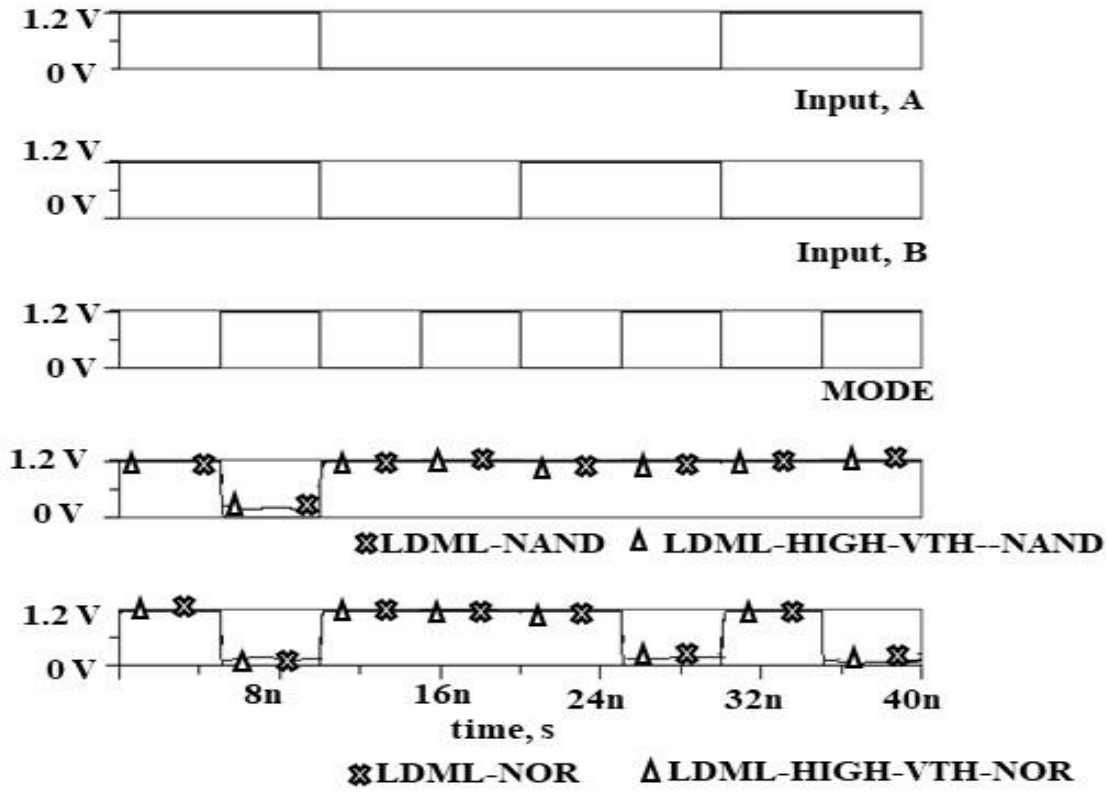



(a)

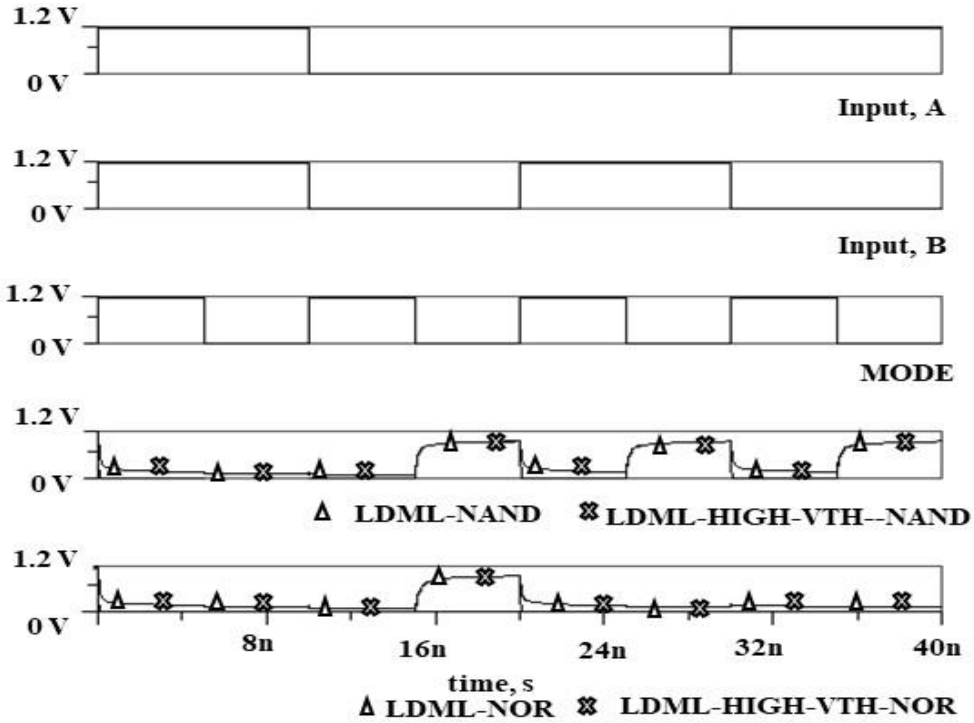



(b)

Fig. 3.3 Transient waveforms of the proposed LDML design in static mode
(a) 2-input type A NAND and NOR gate (b) 2-input type B NAND and NOR gate




(a)




(b)

Fig. 3.4 Transient waveforms of the proposed LDML design in dynamic mode (a) 2-input type A NAND and NOR gate (b) 2-input type B NAND and NOR gate

Further, in order to show the cascading of type A and type B topologies of LDML and LDML-HIGH-VTH designs, a 1-bit FA circuit is also implemented using the schematic shown in Fig. 3.5 [6]. This schematic is realized using footed DML and proposed LDML and LDML-HIGH-VTH designs. The sum block is implemented using type B topology and the carry block is implemented using type A topology.

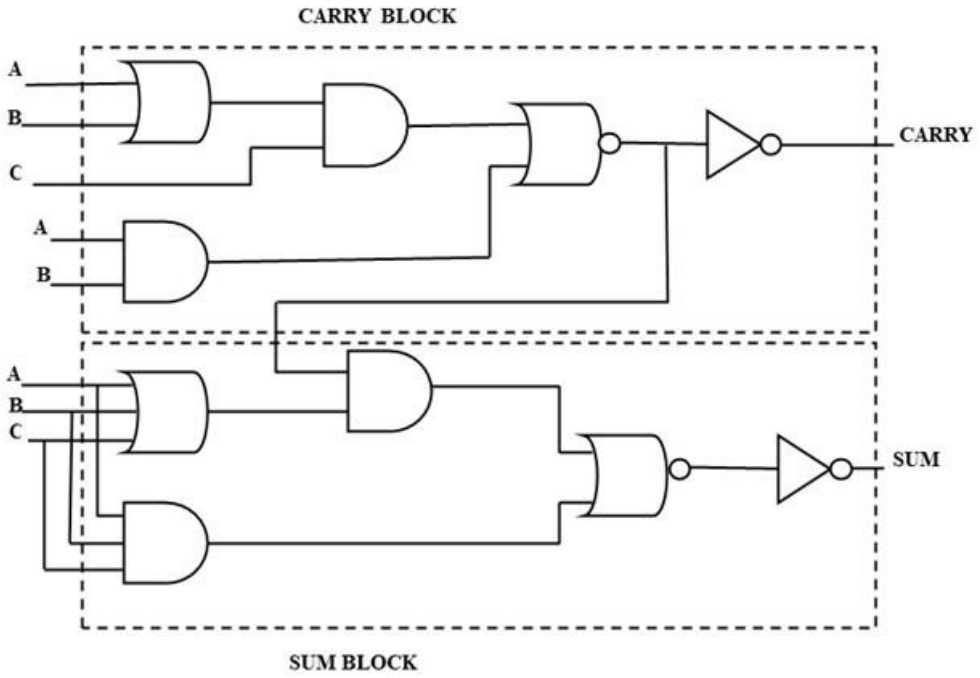
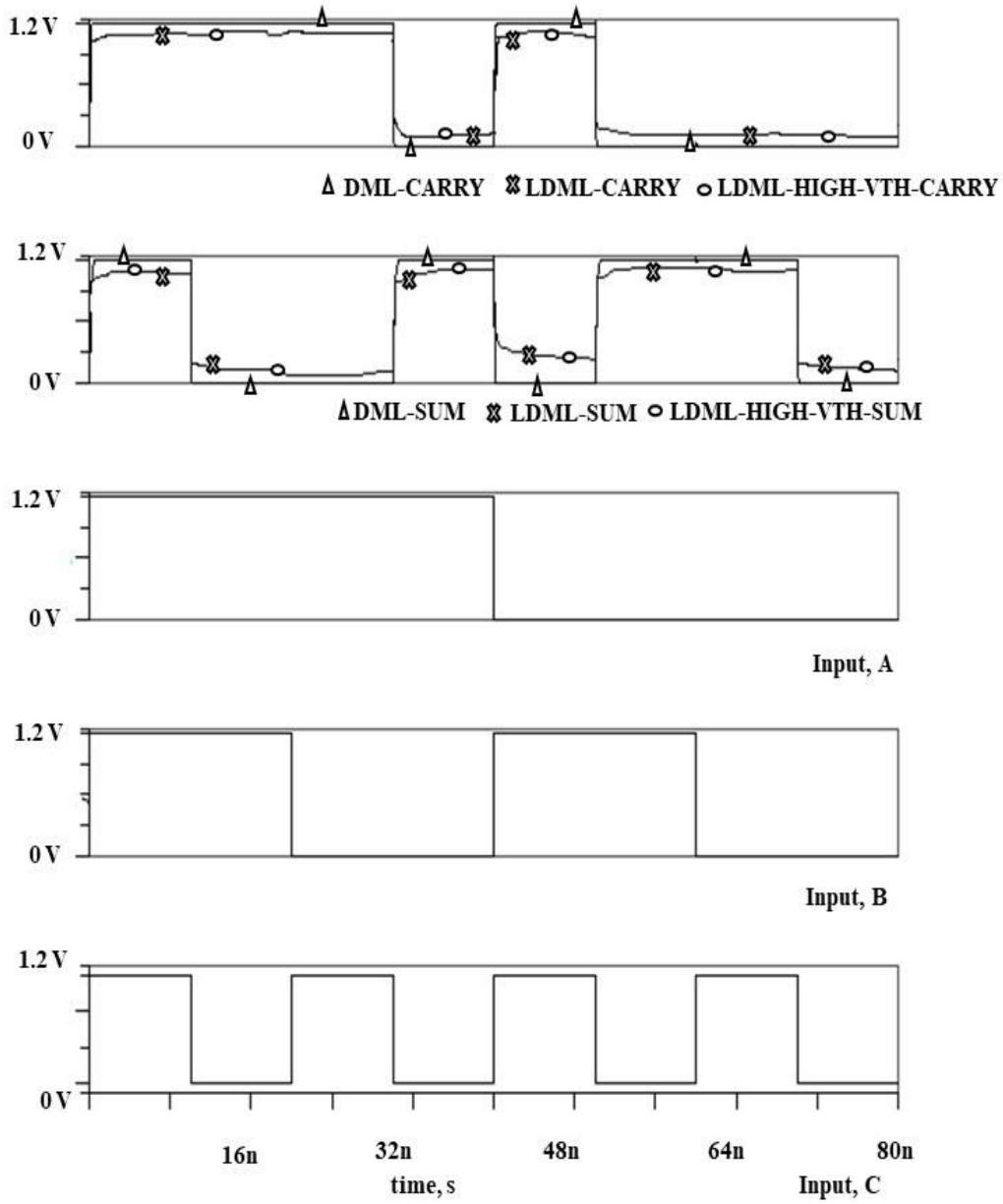


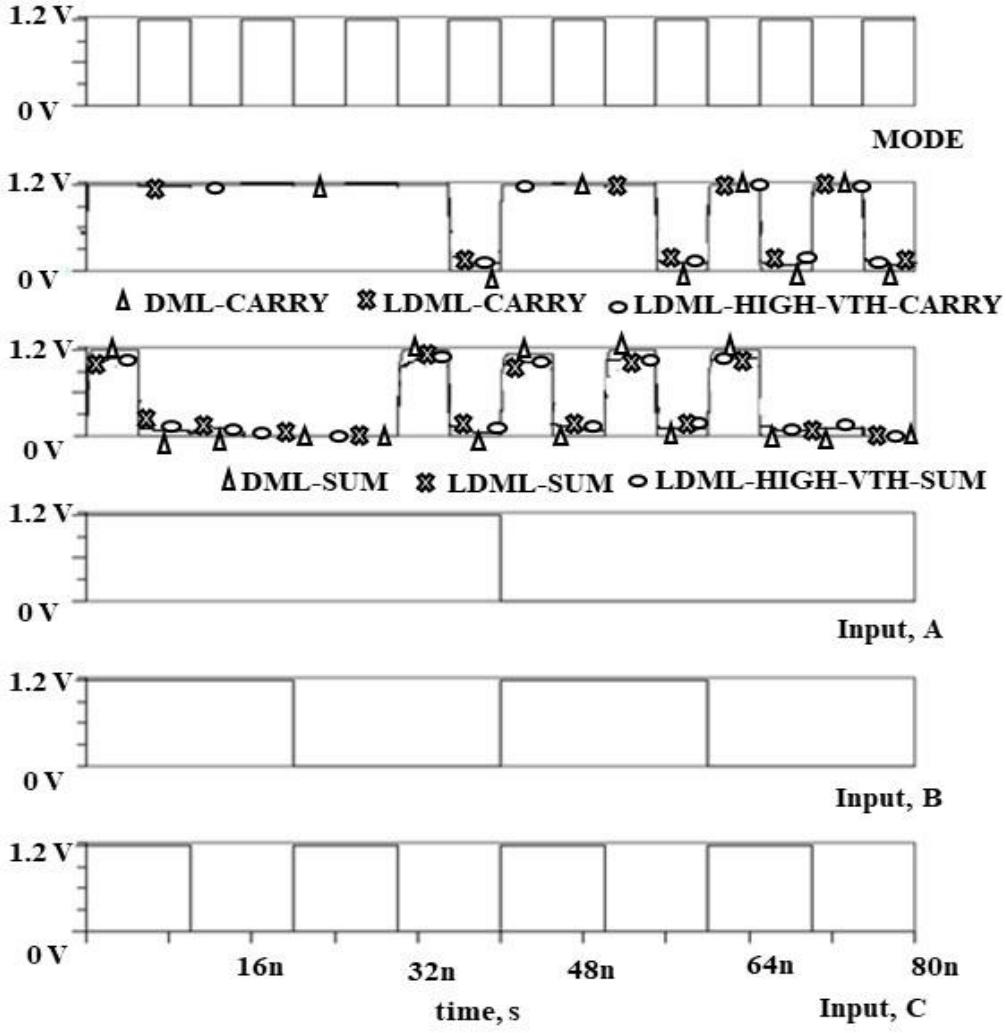

Fig. 3.5 Schematic of a 1-bit FA design [6]

The functional verification of the FA is carried out by applying inputs A, B, C and MODE input as shown in Fig. 3.6. The transient waveforms for sum and carry for DML (DML-SUM, DML-CARRY), LDML (LDML-SUM,LDML-CARRY) and LDML-HIGH-VTH (LDML-HIGH-VTH-SUM,LDML-HIGH-VTH-CARRY) are depicted in Fig. 3.6 (a) and Fig. 3.6 (b) for static and dynamic mode respectively. It may be noted that in static mode, the SUM bit is logic “1” when an odd number of logic “1” among the inputs and the CARRY bit is logic “1” when at least two of the three inputs are logic “1”. In pre-charge/pre-discharge phase of dynamic mode, since the sum block is type B, therefore MODE is logic “1” causing the SUM bit to be at logic “0”. Similarly, since the

carry block is type A therefore MODE is logic “0” as a result the CARRY bit is logic “1”. During the evaluation phase, the SUM bit becomes logic “1” when there's an odd number of logic “1” inputs, while the CARRY bit is logic “1” if at least two out of the three inputs are logic “1”.




(a)




(b)

Fig. 3.6 Transient waveform of proposed LDML based 1-bit FA (a) Static mode (b) Dynamic mode

### 3.3.2.2 Performance comparison

The existing footed DML and proposed LDML designs are compared in static and dynamic mode in terms of leakage power, delay and leakage PDP for proposed LDML and footed DML based 2-input type A and type B NAND and NOR gates and 1-bit FA circuit using Symica DE tool at 1.2 V supply voltage. Table 3.1 enlists the leakage power, delay and leakage PDP of proposed LDML and footed DML based 2-input type A and

type B NAND and NOR gates and 1-bit FA circuit in static mode at 90nm and 45nm.

Following are the observations from Table 3.1:

i. In static mode, the maximum percentage leakage power saving is 30.49% for LDML and 44.85% for LDML-HIGH-VTH at 90nm.

ii. The percentage leakage power saving increases with technology scaling, the corresponding values are 57.32% for LDML and 66.61% for LDML-HIGH-VTH at 45nm .

iii. The proposed LDML based gates show increased delay in comparison to DML counterparts which may be attributed to the LCTs placed between PUN and PDN networks.

iv. The proposed LDML-HIGH-VTH design offers better leakage power saving than proposed LDML design.

Table 3.1 Leakage power, delay and leakage PDP of proposed LDML and footed DML based 2-input type A and type B NAND and NOR gates and 1-bit FA circuit in static mode at 90nm and 45nm at 27℃

| | Circuit | Leakage Power(nW) | | | Delay(ns) | | | Leakage PDP (aJ) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 90nm | | Footed DML | LDML | LDML-HIGH-VTH | Footed DML | LDML | LDML-HIGH-VTH | Footed DML | LDML | LDML-HIGH-VTH |
| | TA-NAND2 | 25.6 | 19.37 | 15.78 | 0.07 | 0.08 | 0.09 | 1.79 | 1.55 | 1.42 |
| | TB-NAND2 | 39.42 | 27.52 | 21.74 | 0.09 | 0.1 | 0.11 | 3.55 | 2.75 | 2.39 |
| | TA-NOR2 | 34.45 | 26.08 | 21.23 | 0.09 | 0.1 | 0.11 | 3.1 | 2.61 | 2.34 |
| | TB-NOR2 | 26.57 | 18.47 | 14.66 | 0.11 | 0.13 | 0.14 | 2.92 | 2.4 | 2.05 |
| | FA | 244.95 | 189.69 | 181.06 | 0.23 | 0.25 | 0.29 | 56.34 | 47.42 | 52.51 |
| 45nm | | | | | | | | | | |
| | TA-NAND2 | 133.91 | 68.3 | 55 | 0.05 | 0.06 | 0.07 | 6.7 | 4.1 | 3.85 |
| | TB-NAND2 | 205.21 | 88.75 | 68.89 | 0.07 | 0.08 | 0.09 | 14.36 | 7.1 | 6.2 |
| | TA-NOR2 | 184.91 | 94.69 | 76.76 | 0.07 | 0.08 | 0.09 | 12.94 | 7.57 | 6.91 |
| | TB-NOR2 | 135.93 | 58.02 | 45.39 | 0.08 | 0.1 | 0.11 | 10.87 | 5.8 | 4.99 |
| | FA | 974.49 | 720.848 | 679.523 | 0.09 | 0.13 | 0.15 | 87.7 | 95.01 | 105.23 |

The leakage power, delay and leakage PDP of the existing and the proposed 2-input footed type A and type B NAND and NOR gates and 1-bit FA in dynamic mode

(pre-charge/pre-discharge and evaluation phase) at 90nm and 45nm is enlisted in Table 3.2. Following are the observations from Table 3.2:

i. During the pre-charge/pre-discharge phase, LDML design results in a maximum percentage leakage power saving of 17.22% at 90nm, and 34.99% at 45nm.

ii. The LDML-HIGH-VTH design results in a maximum percentage leakage power saving of 29.98% at 90nm, and 40.42% at 45nm in pre-charge / pre-discharge phase.

iii. During the evaluation phase in dynamic mode, LDML design results in a maximum percentage leakage power saving of 30.49% at 90nm, and 57.32% at 45nm.

iv. The LDML-HIGH-VTH design results in a maximum percentage leakage power saving of 44.85% at 90nm, and 66.61% at 45nm in evaluation phase.

v. As technology scaling occurs, the amount of power saved from leakage increases using the proposed design.

Table 3.2 Leakage power, delay and leakage PDP of proposed LDML and footed DML based 2-input type A and type B NAND and NOR gates, 1-bit FA circuit in dynamic mode at 90nm and 45nm at 27°C

| | Circuit | Leakage Power(nW) | | | Delay(nS) | | | Leakage PDP(aJ) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 90nm | | Footed DML | LDML | LDML-HIGH-VTH | Footed DML | LDML | LDML-HIGH-VTH | Footed DML | LDML | LDML-HIGH-VTH |
| Pre-charge/ Pre-discharge | TA-NAND2 | 5.88 | 5.61 | 4.75 | 0.03 | 0.04 | 0.05 | 0.18 | 0.22 | 0.24 |
| | TB-NAND2 | 10.12 | 9.26 | 7.47 | 0.05 | 0.07 | 0.09 | 0.51 | 0.65 | 0.67 |
| | TA-NOR2 | 16.38 | 14.94 | 12.24 | 0.02 | 0.04 | 0.05 | 0.33 | 0.6 | 0.61 |
| | TB-NOR2 | 3.36 | 3.21 | 2.76 | 0.06 | 0.07 | 0.09 | 0.2 | 0.22 | 0.25 |
| | FA | 51.34 | 42.5 | 35.95 | 0.11 | 0.12 | 0.15 | 5.65 | 5.1 | 5.39 |
| Evaluation | TA-NAND2 | 25.6 | 19.36 | 15.78 | 0.03 | 0.04 | 0.05 | 0.77 | 0.77 | 0.79 |
| | TB-NAND2 | 39.42 | 27.52 | 21.74 | 0.05 | 0.07 | 0.09 | 1.97 | 1.93 | 1.96 |
| | TA-NOR2 | 34.48 | 26.08 | 21.24 | 0.02 | 0.04 | 0.05 | 0.69 | 1.04 | 1.06 |
| | TB-NOR2 | 26.57 | 18.47 | 14.66 | 0.06 | 0.07 | 0.09 | 1.59 | 1.29 | 1.32 |
| | FA | 244.95 | 189.69 | 181.06 | 0.11 | 0.12 | 0.15 | 26.94 | 22.76 | 27.16 |
| 45nm | | | | | | | | | | |
| Pre-charge/ Pre-discharge | TA-NAND2 | 20.34 | 18.51 | 16.19 | 0.02 | 0.03 | 0.04 | 0.41 | 0.56 | 0.65 |
| | TB-NAND2 | 32.25 | 26.59 | 21.76 | 0.03 | 0.04 | 0.05 | 0.97 | 1.06 | 1.09 |
| | TA-NOR2 | 61.79 | 52.36 | 44.17 | 0.01 | 0.02 | 0.03 | 0.62 | 1.05 | 1.33 |
| | TB-NOR2 | 8.96 | 8.22 | 7.22 | 0.04 | 0.04 | 0.05 | 0.36 | 0.33 | 0.36 |
| | FA | 188.81 | 122.74 | 112.49 | 0.05 | 0.05 | 0.06 | 9.44 | 6.14 | 6.75 |
| Evaluation | TA-NAND2 | 133.91 | 68.3 | 55 | 0.02 | 0.03 | 0.04 | 2.68 | 2.05 | 2.2 |
| | TB-NAND2 | 205.21 | 88.75 | 68.89 | 0.03 | 0.04 | 0.05 | 6.16 | 3.55 | 3.44 |
| | TA-NOR2 | 184.91 | 94.69 | 76.76 | 0.01 | 0.02 | 0.03 | 1.85 | 1.89 | 2.3 |
| | TB-NOR2 | 135.93 | 58.02 | 45.39 | 0.04 | 0.04 | 0.05 | 5.44 | 2.32 | 2.27 |
| | FA | 974.49 | 730.85 | 701.52 | 0.05 | 0.05 | 0.06 | 48.72 | 36.54 | 42.09 |

Further, the efficiency of the proposed technique in terms of percentage leakage power saving is investigated at different temperatures i.e. -25 °C, 27 °C and 100 °C at 90nm and 45nm in static and dynamic mode. In static mode, the percentage leakage power saving achieved for 2-input type A and type B NAND and NOR gates and 1-bit FA for -25 °C, 27 °C and 100 °C at 90nm and 45nm is enlisted in Tables 3.3 and 3.4 respectively. Following are the observations from Tables 3.3 and 3.4:

i. The results demonstrate that the leakage power in LDML design is reduced as compared to footed DML design in static mode.
ii. Percentage leakage power saving varies from 25.18% to 50.58% and 39.48% to 70.37% for 90nm and 45nm respectively at -25℃.
iii. Percentage leakage power saving decreases to 22.56% to 44.84% for 90nm and 26.03% to 66.6% for 45nm at 27℃.
iv. Percentage leakage power saving is 18.54% to 41.79% for 90nm and by 23.2% to 63.36% for 45nm at 100℃.

Table 3.3 Percentage leakage power saving for 2-input type A and type B NAND and NOR gates, 1-bit FA circuit in static mode for different temperature at 90nm

| 90nm Process Technology, Supply Voltage =1.2 V, Static Mode of DML | | | | | | |
|---|---|---|---|---|---|---|
| Circuit | Percentage leakage power saving at -25℃ | | Percentage leakage power saving at 27℃ | | Percentage leakage power saving at 100℃ | |
| | LDML | LDML-HIGH-VTH | LDML | LDML-HIGH-VTH | LDML | LDML-HIGH-VTH |
| TA-NAND2 | 28.56 | 44.68 | 24.37 | 38.36 | 21.66 | 33.49 |
| TB-NAND2 | 34.06 | 50.58 | 30.19 | 44.84 | 27.98 | 40.78 |
| TA-NOR2 | 28.52 | 44.28 | 24.31 | 38.38 | 21.98 | 33.72 |
| TB-NOR2 | 33.34 | 49.46 | 30.48 | 44.82 | 29.29 | 41.79 |
| FA | 25.18 | 33.27 | 22.56 | 26.08 | 18.54 | 23.91 |

Table 3.4 Percentage leakage power saving for 2-input type A and type B NAND and NOR gates, 1-bit FA circuit in static mode for different temperature at 45nm

| 45nm Process Technology, Supply Voltage =1.2 V, Static Mode of DML | | | | | | |
|---|---|---|---|---|---|---|
| Circuit | Percentage leakage power saving at -25℃ | | Percentage leakage power saving at 27℃ | | Percentage leakage power saving at 100℃ | |
| | LDML | LDML-HIGH-VTH | LDML | LDML-HIGH-VTH | LDML | LDML-HIGH-VTH |
| TA-NAND2 | 54.09 | 64.18 | 48.99 | 58.93 | 44.53 | 53.59 |
| TB-NAND2 | 60.38 | 70.37 | 56.75 | 66.43 | 53.27 | 62.35 |
| TA-NOR2 | 53.41 | 63.15 | 48.79 | 58.49 | 44.59 | 53.54 |
| TB-NOR2 | 59.79 | 69.55 | 57.32 | 66.6 | 54.73 | 63.36 |
| FA | 39.48 | 49.22 | 26.03 | 30.27 | 23.2 | 27.46 |

In dynamic mode, the percentage leakage power saving achieved for footed DML designs for type A and type B topology for -25 °C, 27 °C and 100 °C at 90nm and 45nm is enlisted in Tables 3.5 and 3.6, respectively. Following are the observations from Tables 3.5 and 3.6:

i. The results demonstrate that the leakage power in LDML circuits is reduced as compared to footed DML circuits across different temperature in dynamic mode.
ii. At -25℃, percentage leakage power saving is 4.12% to 50.58% for 90nm and 9.08% to 70.37% for 45nm;
iii. At 27℃, percentage leakage power saving is 4.38% to 44.84% for 90nm and 8.28% to 66.6% for 45nm.
iv. At 100℃, percentage leakage power saving is 3.09% to 41.79% for 90nm and 6.41% to 63.36% for 45nm.

Table 3.5 Percentage leakage power saving for 2-input type A and type B NAND and NOR gates, 1-bit FA circuit in dynamic mode for different temperature at 90nm

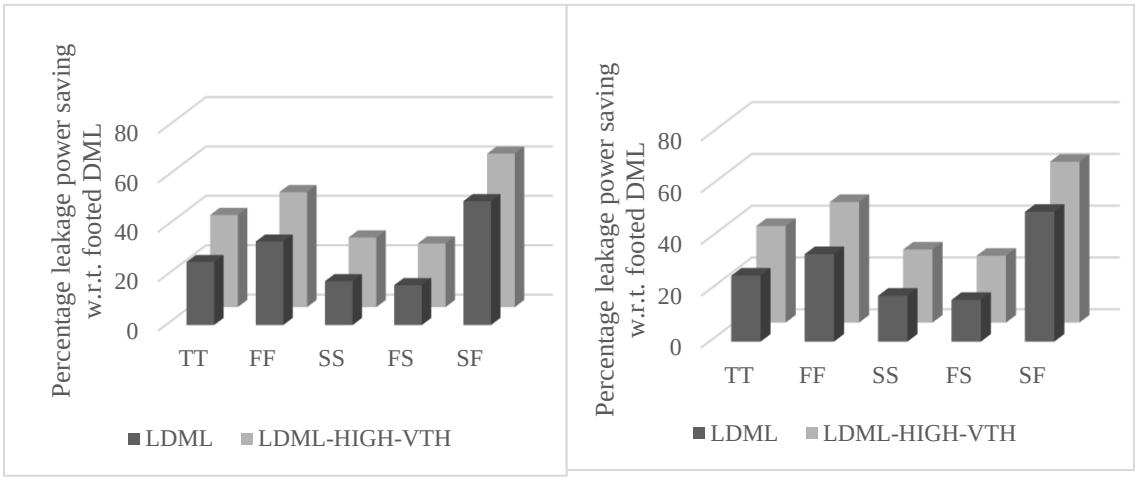
| 90nm Process Technology, Supply Voltage =1.2 V, Dynamic Mode of DML | | | | | | |
|---|---|---|---|---|---|---|
| | Percentage leakage power saving at -25℃ | | Percentage leakage power saving at 27℃ | | Percentage leakage power saving at 100℃ | |
| Pre-charge/ Pre-discharge | LDML | LDML-HIGH-VTH | LDML | LDML-HIGH-VTH | LDML | LDML-HIGH-VTH |
| TA-NAND2 | 10.39 | 30.86 | 4.51 | 19.24 | 3.09 | 12.98 |
| TB-NAND2 | 9.03 | 29.7 | 8.55 | 26.26 | 8.27 | 23.27 |
| TA-NOR2 | 14.75 | 35.16 | 8.79 | 25.24 | 6.82 | 19.89 |
| TB-NOR2 | 4.12 | 20.71 | 4.38 | 17.67 | 3.85 | 14.79 |
| FA | 18.1 | 31.34 | 17.2 | 29.97 | 16.72 | 21.53 |
| Evaluation | | | | | | |
| TA-NAND2 | 28.56 | 44.68 | 24.37 | 38.36 | 21.66 | 33.49 |
| TB-NAND2 | 34.06 | 50.58 | 30.19 | 44.84 | 27.98 | 40.78 |
| TA-NOR2 | 28.52 | 44.28 | 24.31 | 38.38 | 21.98 | 33.72 |
| TB-NOR2 | 33.34 | 49.46 | 30.48 | 44.82 | 29.29 | 41.79 |
| FA | 25.18 | 33.27 | 22.56 | 26.08 | 18.54 | 23.91 |

Table 3.6 Percentage leakage power saving for 2-input type A and type B NAND and NOR gates, 1-bit FA circuit in dynamic mode for different temperature at 45nm

| 45nm Process Technology, Supply Voltage =1.2 V, Dynamic Mode of DML | | | | | | |
|---|---|---|---|---|---|---|
| | Percentage leakage power saving at -25℃ | | Percentage leakage power saving at 27℃ | | Percentage leakage power saving at 100℃ | |
| Pre-charge/ Pre-discharge | LDML | LDML-HIGH-VTH | LDML | LDML-HIGH-VTH | LDML | LDML-HIGH-VTH |
| TA-NAND2 | 16.69 | 29.66 | 9.03 | 20.41 | 6.41 | 15.37 |
| TB-NAND2 | 18.71 | 35.65 | 17.55 | 32.53 | 16.81 | 30.07 |
| TA-NOR2 | 21.24 | 35.68 | 15.26 | 28.51 | 12.82 | 24.27 |
| TB-NOR2 | 9.08 | 20.96 | 8.28 | 19.36 | 8.14 | 17.82 |
| FA | 36.33 | 43.12 | 34.99 | 40.42 | 29.21 | 31.54 |
| Evaluation | | | | | | |
| TA-NAND2 | 54.09 | 64.18 | 48.99 | 58.93 | 44.53 | 53.59 |
| TB-NAND2 | 60.38 | 70.37 | 56.75 | 66.43 | 53.27 | 62.35 |
| TA-NOR2 | 53.41 | 63.15 | 48.79 | 58.49 | 44.59 | 53.54 |
| TB-NOR2 | 59.79 | 69.55 | 57.32 | 66.6 | 54.73 | 63.36 |
| FA | 39.48 | 49.22 | 26.03 | 30.27 | 23.2 | 27.46 |

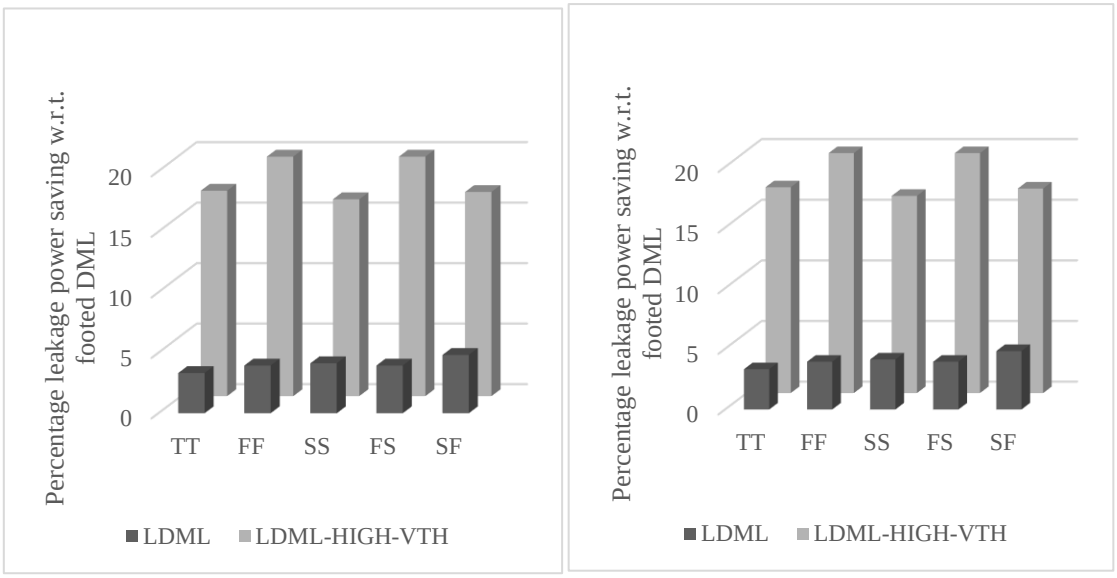
Further, the robustness of the proposed LDML design is checked by considering a 2-input type A NAND gate and analysing it at five different process corners i.e., TT, FF, SS, FS, SF.

Figure 3.7, Figure 3.8 and Figure 3.9 depict the percentage leakage power saving for the proposed LDML based 2-input type A NAND gate compared to the existing footed DML counterpart across five distinct process corners in static mode, pre-charge and evaluation phases of dynamic mode respectively. In static mode, a maximum percentage leakage power saving of 50.14% and 62.14% for LDML and LDML-HIGH-VTH respectively for both 90nm and 45nm. In pre-charge phase of dynamic mode, corresponding values are 4.82 % and 19.79 %. In evaluation phase, LDML shows a maximum percentage leakage power saving of 50.14%, and LDML-HIGH-VTH displays a percentage leakage power saving of 62.14% for both 90nm and 45nm. It can be deduced that the proposed design-I effectively reduces leakage power across all process corners in both static and dynamic mode.



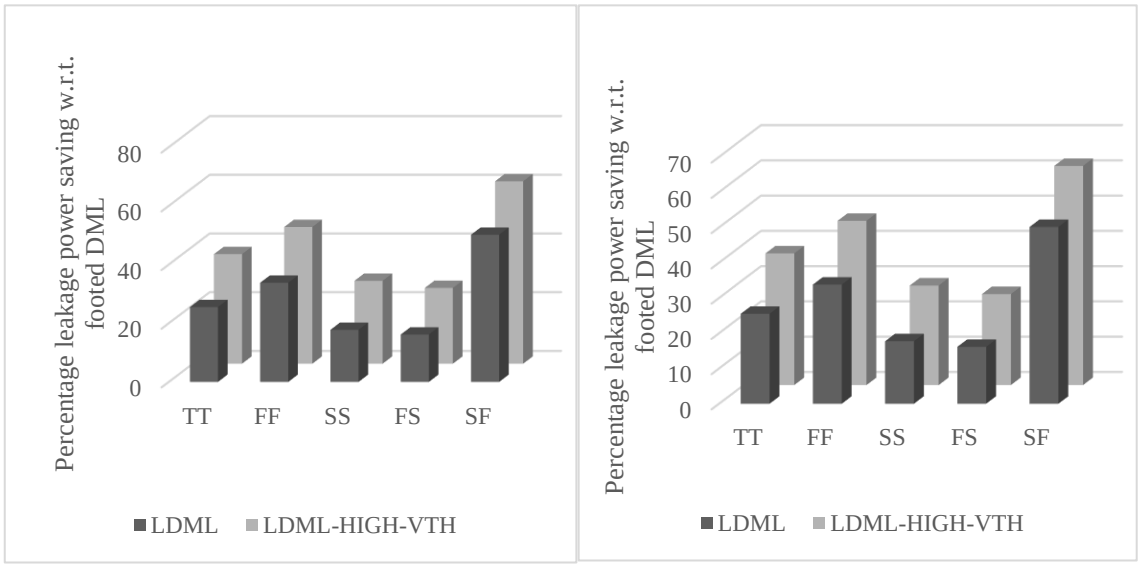

(a) (b)

Fig. 3.7 Percentage leakage power saving for proposed LDML based 2-input type A NAND gate at five different process corners in static mode at (a) 90nm (b) 45nm




(a) (b)

Fig. 3.8 Percentage leakage power saving for proposed LDML based 2-input type A NAND gate at five different process corners in pre-charge phase of dynamic mode at (a) 90nm (b) 45nm

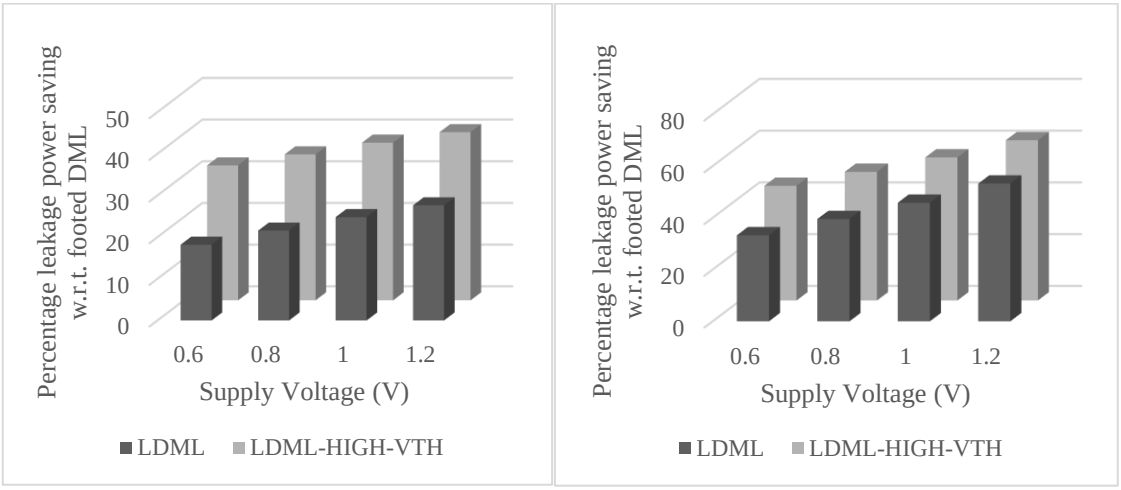



(a) (b)

Fig. 3.9 Percentage leakage power saving for proposed LDML based 2-input type A NAND gate at five different process corners in evaluation phase of dynamic mode at (a) 90nm (b) 45nm

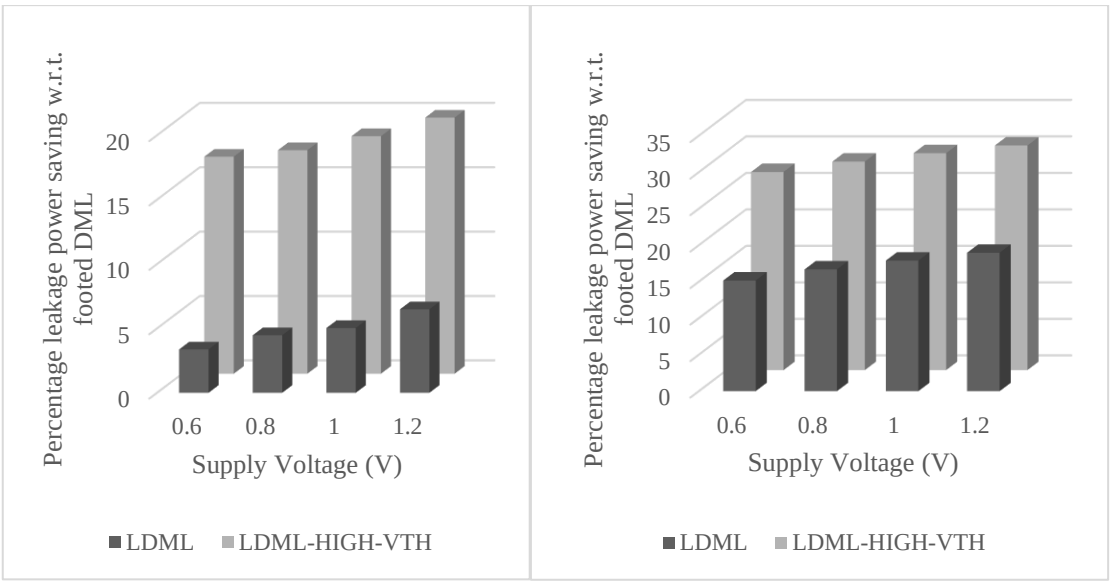
The efficacy of the proposed LDML design is also investigated for 2-input type A NAND gate at different supply voltages (0.6 V-1.2 V) at 90nm and 45nm.

Figure 3.10, Figure 3.11 and Figure 3.12 illustrates the percentage leakage power saving achieved using LDML and LDML-HIGH-VTH design in static, pre-charge phase of dynamic mode and evaluation phase of dynamic mode respectively. It may be noted that the proposed design-I is efficient at all supply voltages in both static and dynamic mode at 90nm and 45nm with maximum percentage leakage power saving of 27.64% and 40.35% at 90nm and 53.22% and 61.91% at 45nm for LDML and LDML-HIGH-VTH design respectively, in static mode. The corresponding values are 6.49% and 19.89% at 90nm and 18.97% and 30.77% at 45nm in pre-charge phase of dynamic mode. In evaluation phase, a maximum percentage leakage power saving of 27.64% and 40.35% at 90nm and 53.22% and 61.91% at 45nm for LDML and LDML-HIGH-VTH design respectively.



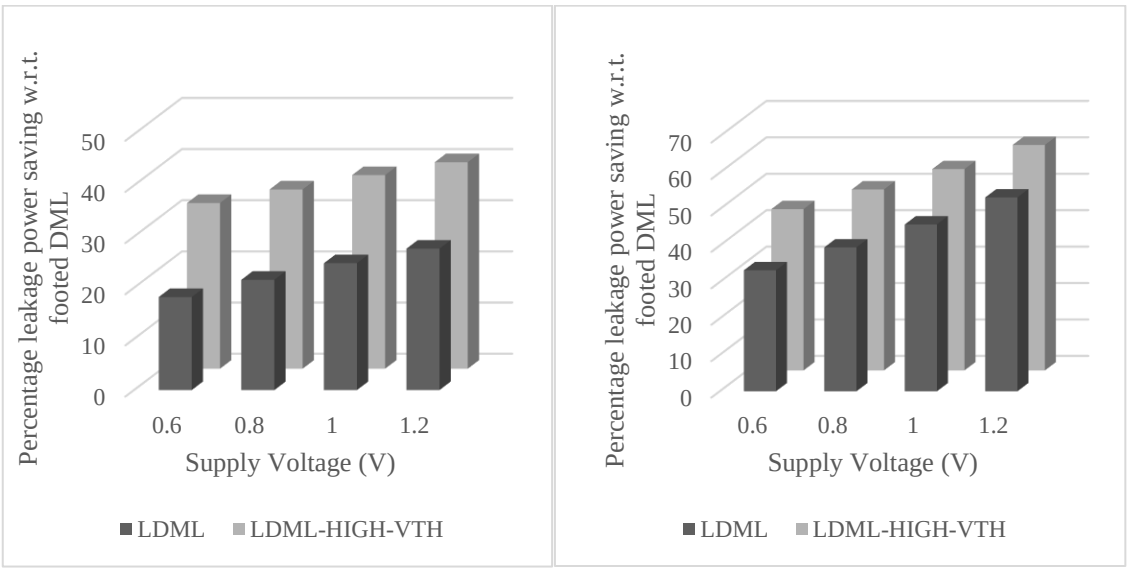

(a) (b)

Fig. 3.10 Percentage leakage power saving for proposed LDML based 2-input type A NAND gate at different voltages in static mode at (a) 90nm (b) 45nm




(a) (b)

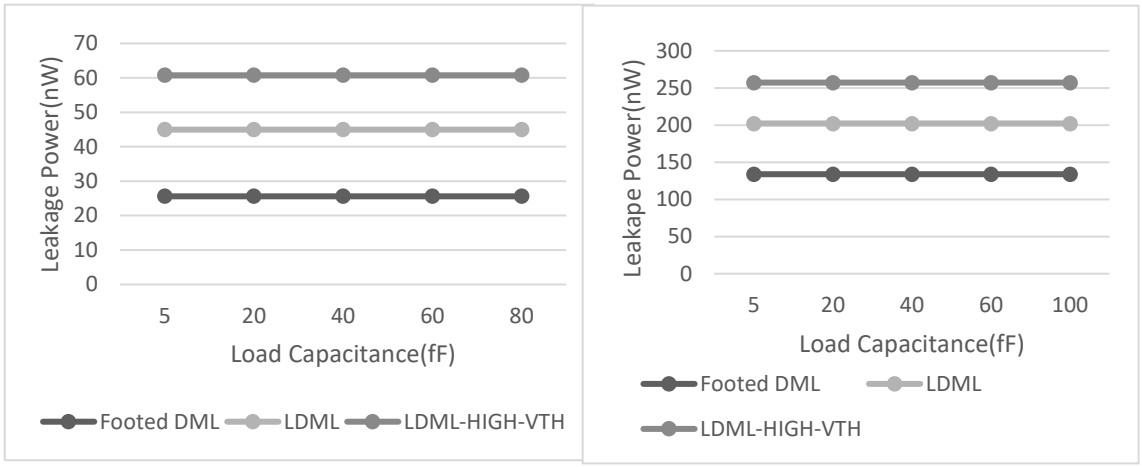
Fig. 3.11 Percentage leakage power saving for proposed LDML based 2-input type A NAND gate at different voltages in pre-charge phase of dynamic mode at (a) 90nm (b) 45nm




(a) (b)

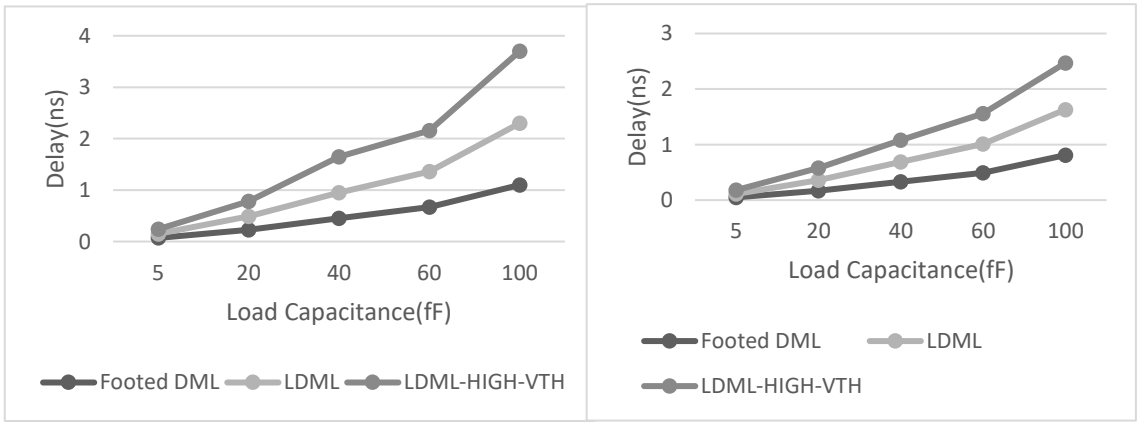
Fig. 3.12 Percentage leakage power saving for proposed LDML based 2-input type A NAND gate at different voltages in evaluation phase of dynamic mode at (a) 90nm (b) 45nm

Further, the variation in leakage power and delay is also observed for LDML based 2-input type A NAND gate by varying load capacitor (5fF-100fF) at 90nm and 45nm as depicted in Fig. 3.13 and 3.14, respectively. It may be observed that with increase in load capacitance value, the leakage power remains constant. However, there is an increase in delay value with increase in load capacitance and the effect is more severe in case of LDML-HIGH-VTH as compared to LDML design.




(a) (b)

Fig. 3.13 Effect of variation of load capacitance on leakage power for LDML based 2-input type A NAND gate (a) 90nm (b) 45nm




(a) (b)

Fig. 3.14 Effect of variation of load capacitance on delay for LDML based 2-input type A NAND gate (a) 90nm (b) 45nm

Few of the observations which have been made from Tables 3.1-3.6 are:

i. As the design progresses towards lower technology node i.e., from 90nm to 45nm, leakage power of the design increases.

ii. The efficacy of the proposed LDML design in mitigating leakage power increases as technology scales.

iii. When LDML design is implemented with high threshold voltage for LCTs then there is an increase in percentage leakage power saving of the design as compared to the standard VTH design.

iv. For a 1-bit FA, significant percentage leakage power saving is witnessed using the proposed designs. Similar to the smaller designs, the proposed LDML with high VTH design is more effective in combating leakage power as compared to LDML with standard VTH design.

## 3.4 Proposed Design-II: GALEOR based DML logic (GDML) and GALEOR based DML logic with footed Diode (GDMLD)

The leakage reduction in existing type A and type B footed DML designs can also be achieved using the existing GALEOR leakage reduction technique. The proposed design-II- both GDML and GDMLD modify the existing footed DML design by incorporating additional GLT transistors ($GLT_1$, $GLT_2$). An additional footed diode transistor is used in GDML design yielding GDMLD design. The proposed designs achieve leakage reduction by using the concept of stacking in footed DML design.

### 3.4.1 Operation

The proposed GDML design incorporates GLTs in footed DML design. Figure 3.15 depicts the proposed GDML type A NAND gate (GDML-TA-NAND) and GDML type B NAND gate (GDML-TB-NAND). Here $GLT_1$ (NMOS)and $GLT_2$ (PMOS)

are introduced in footed DML type A and type B NAND gate, shown in Fig. 3.1. It may be noted that the drain and gate terminals of each GLT are connected. The source of both $GLT_1$ and $GLT_2$ are connected to the output node.

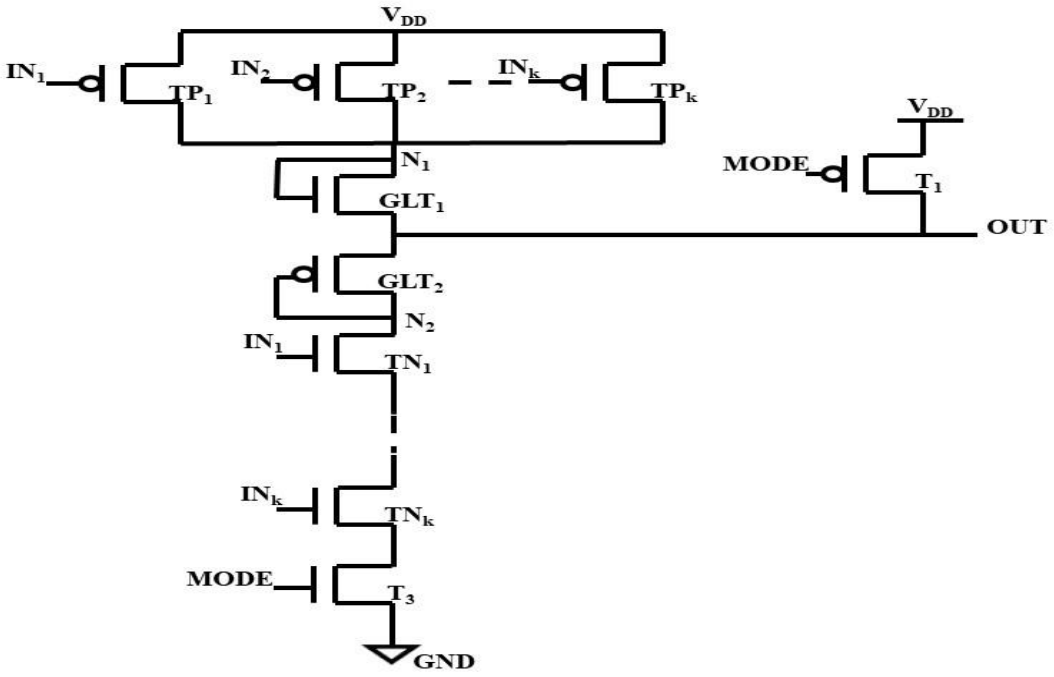
In static mode of proposed GDML type A NAND gate, the MODE input is constant logic "1". Therefore, transistor $T_1$ is off while footer transistor $T_3$ is in on condition. The output of the gate depends on applied inputs. If all inputs are logic "1", then transistors $TN_1$-$TN_k$ are on and $TP_1$-$TP_k$ remain off. Transistor $GLT_1$ is off and $GLT_2$ is on. Therefore, the output attains logic "0" value. Due to presence of off $GLT_1$ transistor in the path from supply voltage to ground, the effective resistance increases along the path, which results in less leakage current. Further, when all inputs are set logic "0", then transistors $TN_1$-$TN_k$ are off and $TP_1$-$TP_k$ remain on. Transistor $GLT_1$ is on and $GLT_2$ is off. Therefore, the output attains logic "1" value. Due to presence of off $GLT_2$ transistor in the path from supply voltage to ground, the effective resistance increases along the path, which results in less leakage current.

The operation of proposed GDML type A NAND gate in dynamic mode is elucidated here. A clock signal is applied to the MODE input allowing two phases- pre-charge and evaluation. During pre-charge phase, MODE input is logic "0". Therefore, output node is charged to $V_{DD}$ through transistor $T_1$ irrespective of the applied inputs. However, the leakage current depends on the inputs applied. The status of GLTs is similar to that of static mode. The presence of GLTs increases the effective resistance from supply voltage to ground, leading to a reduction in leakage current.

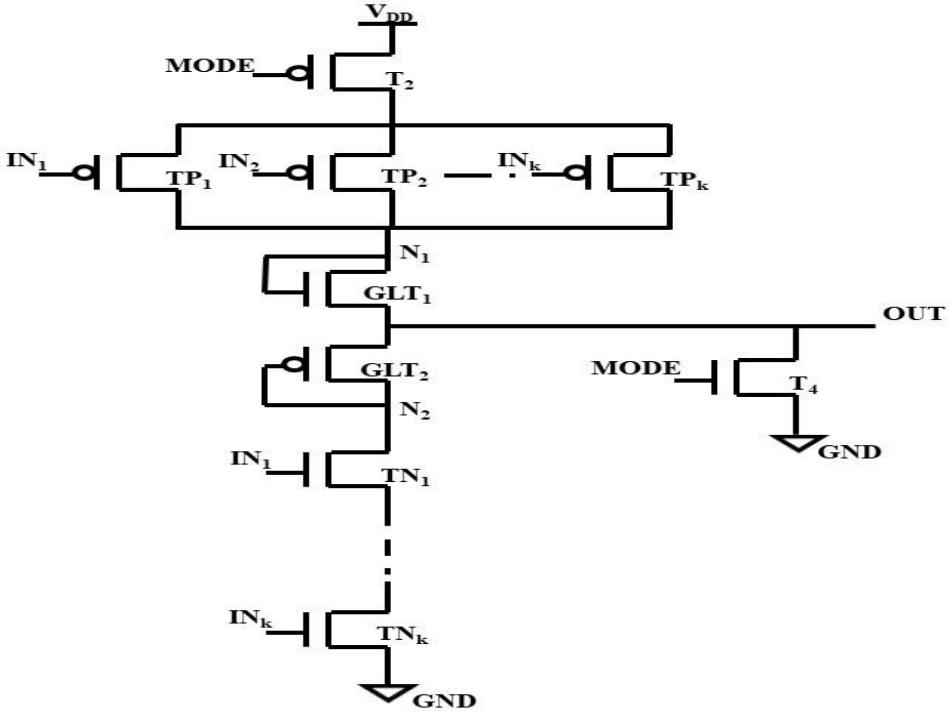
In evaluation phase, the MODE input is logic "1" which makes transistor $T_1$ off and footer transistor $T_3$ on. The output is evaluated according to the inputs applied. When all inputs are logic "1", transistors $TN_1$-$TN_k$ are turned on while $TP_1$-$TP_k$ remain off. As a result, transistor $GLT_1$ is off while $GLT_2$ remains on, causing the output to be at a logic

"0" value. The presence of the off $GLT_1$ transistor in the path from the supply voltage to ground increases the effective resistance along the path, resulting in reduced leakage current. On the contrary, when all inputs are set to logic "0", transistors $TN_1$-$TN_k$ are turned off while $TP_1$-$TP_k$ remain on. This causes transistor $GLT_1$ to be turned on while $GLT_2$ is off, resulting in the output attaining a logic "1" value. The presence of the off $GLT_2$ transistor in the path from the supply voltage to ground increases the effective resistance along the path, which in turn reduces the leakage current.

The proposed GDML type B NAND is shown in Fig. 3.15 (b) and the leakage mechanism is same as that of GDML type A NAND gate. The only difference is that here, in static mode, the MODE input is constant logic "0". Therefore, transistor $T_4$ is off while header transistor $T_2$ is in on condition. In dynamic mode, for pre-discharge phase, MODE input is at logic "1" which makes transistor $T_4$ on and header transistor $T_2$ off. The output is pre-discharged to ground. For evaluation phase, the MODE input is at logic "0", which makes transistor $T_4$ off and header transistor $T_2$ on.




(a)

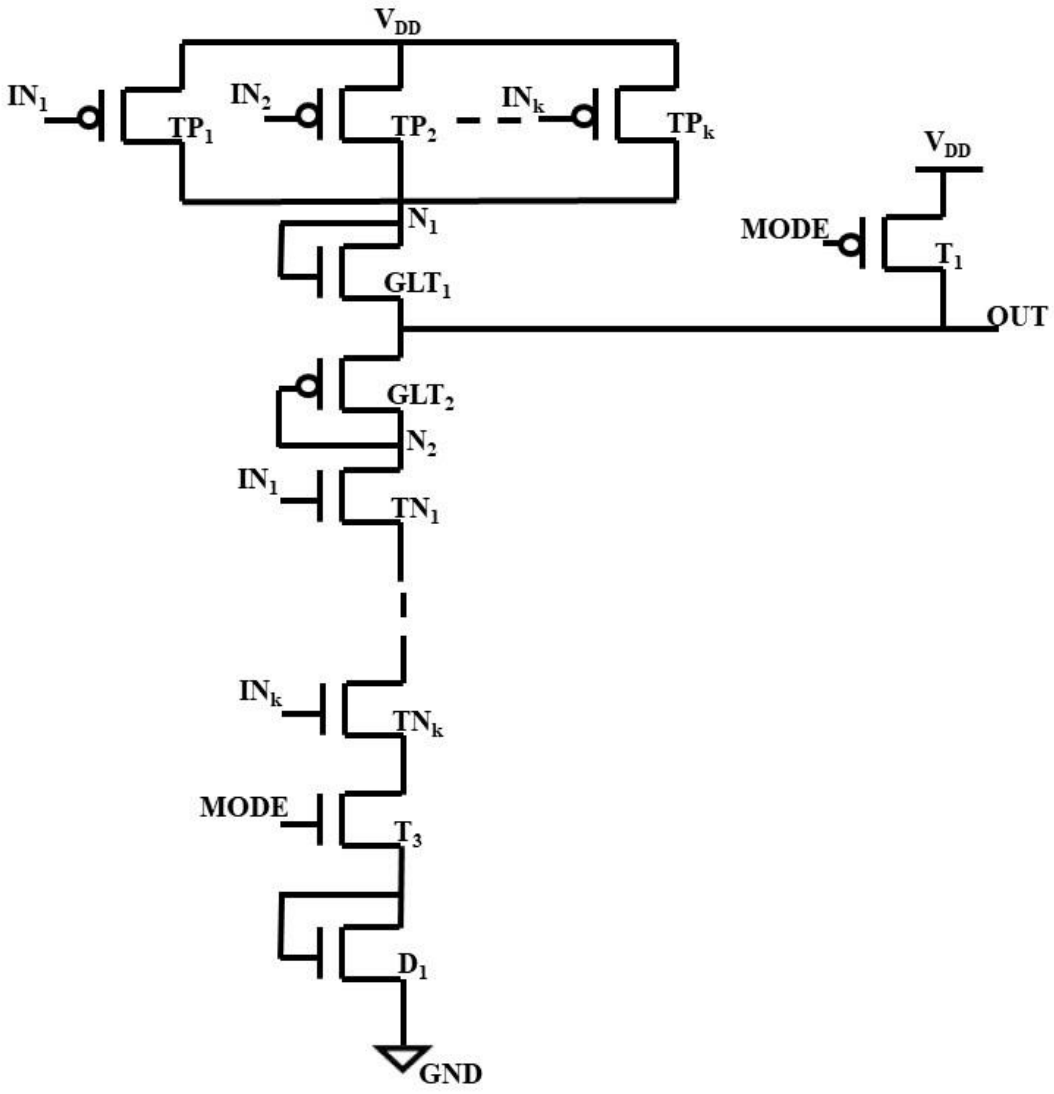



(b)

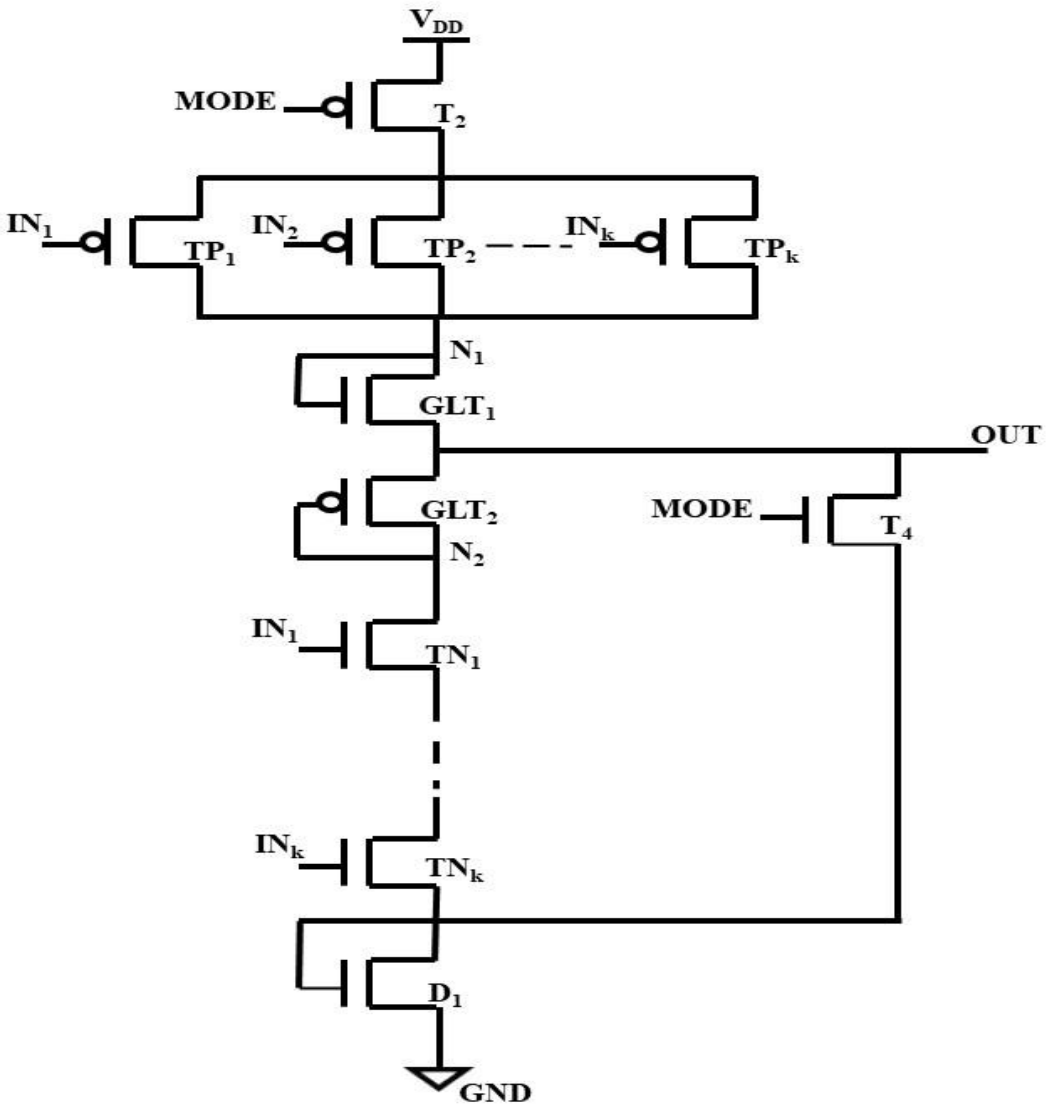
Fig. 3.15 Proposed GDML design (a) Type A NAND gate (b) Type B NAND gate

Further, the GDMLD designs are obtained by placing a footed diode transistor ($D_1$) above the ground terminal in both type A and type B topology designs. The GDML

design of Fig.3.15 is modified by adding an NMOS diode transistor ($D_1$), with its gate and drain terminals connected above the ground terminal. The resulting type A and type B GDMLD designs are shown in Fig. 3.16. This configuration results in further leakage reduction by introducing stacking effect [78]. Here the mechanism behind leakage reduction is same as in the case of GDML designs of type A and type B topology, both in static and dynamic mode.




(a)




(b)

Fig. 3.16 Proposed GDMLD design (a) Type A NAND gate (b) Type B NAND gate

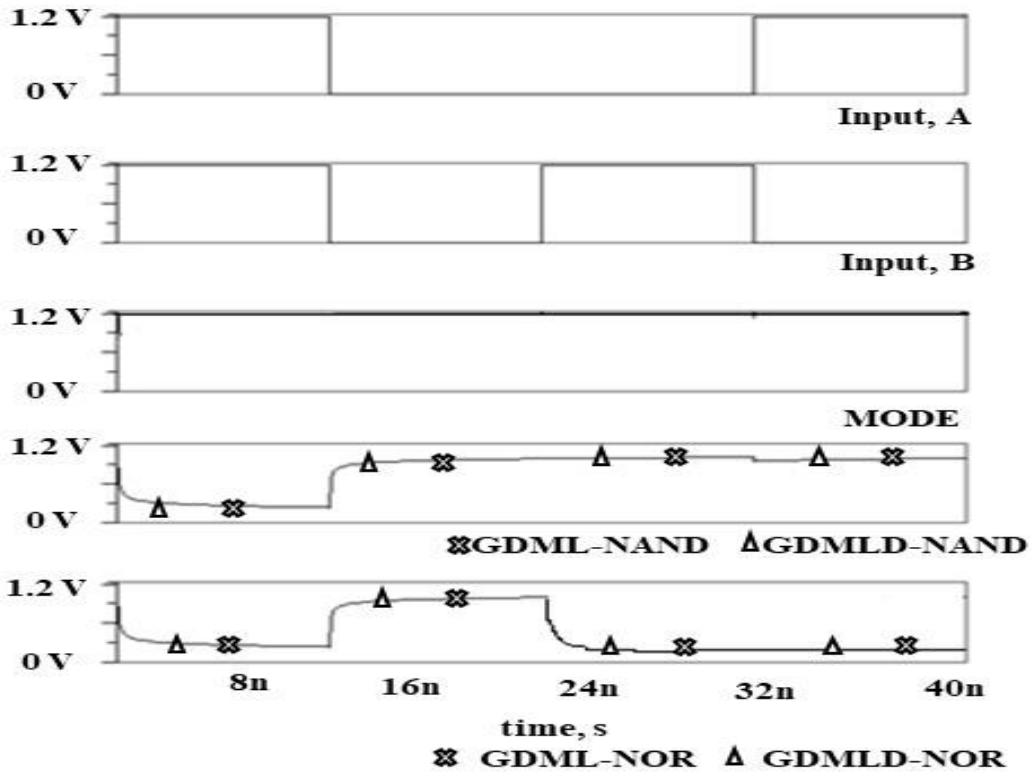
### 3.4.2 Simulation results

This section is divided into two parts- the first part deals with the functional verification while the second part compares the performance of 2-input NAND gate, 2-input NOR gate and 1-bit FA based on proposed GDML and GDMLD designs with corresponding footed DML counterparts. All the circuits are simulated using 90nm and 45nm BSIM4 model card for bulk CMOS with supply voltage of 1.2V and load capacitance of 5fF using Symica DE tool. Corner analysis is also done for 2-input NAND

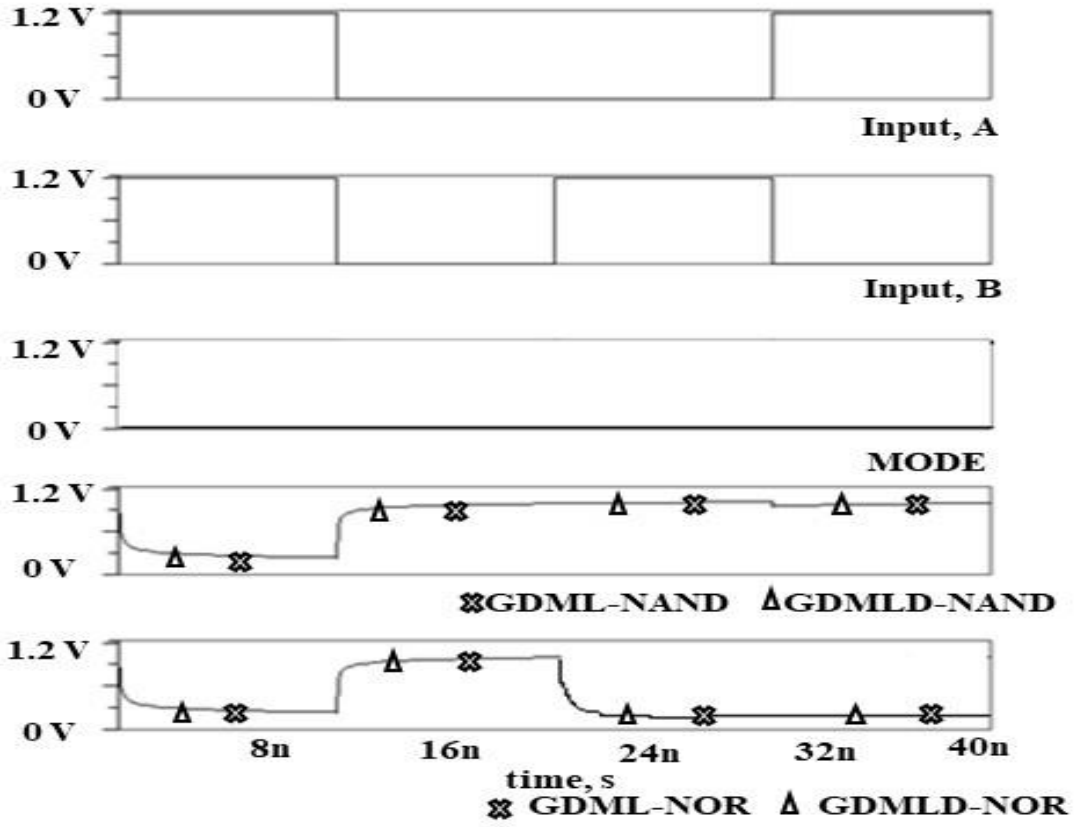
gate. Effect of voltage and temperature variation is also investigated. The SPICE simulator SymSpice is used to demonstrate the operation of proposed designs and SymProbe tool is used for leakage power and delay analysis.

### 3.4.2.1 Functional verification

The 2-input NAND and NOR circuits are implemented using the proposed GDML and GDMLD designs in type A and type B topologies in static and dynamic mode. Figure 3.17 shows the transient waveforms for GDML, GDMLD type A and type B NAND (GDML-NAND,GDMLD-NAND) and NOR gates (GDML-NOR,GDMLD-NOR) in static mode. The MODE input is logic "1" for type A and logic "0" for type B in static mode. It may be noted that output for NAND gate is logic "1" when any of the inputs is logic "0" whereas NOR gate provides output logic "0" when any of the inputs is logic "1". Thus, both GDML and GDMLD based NAND and NOR gates work correctly in static mode.




(a)

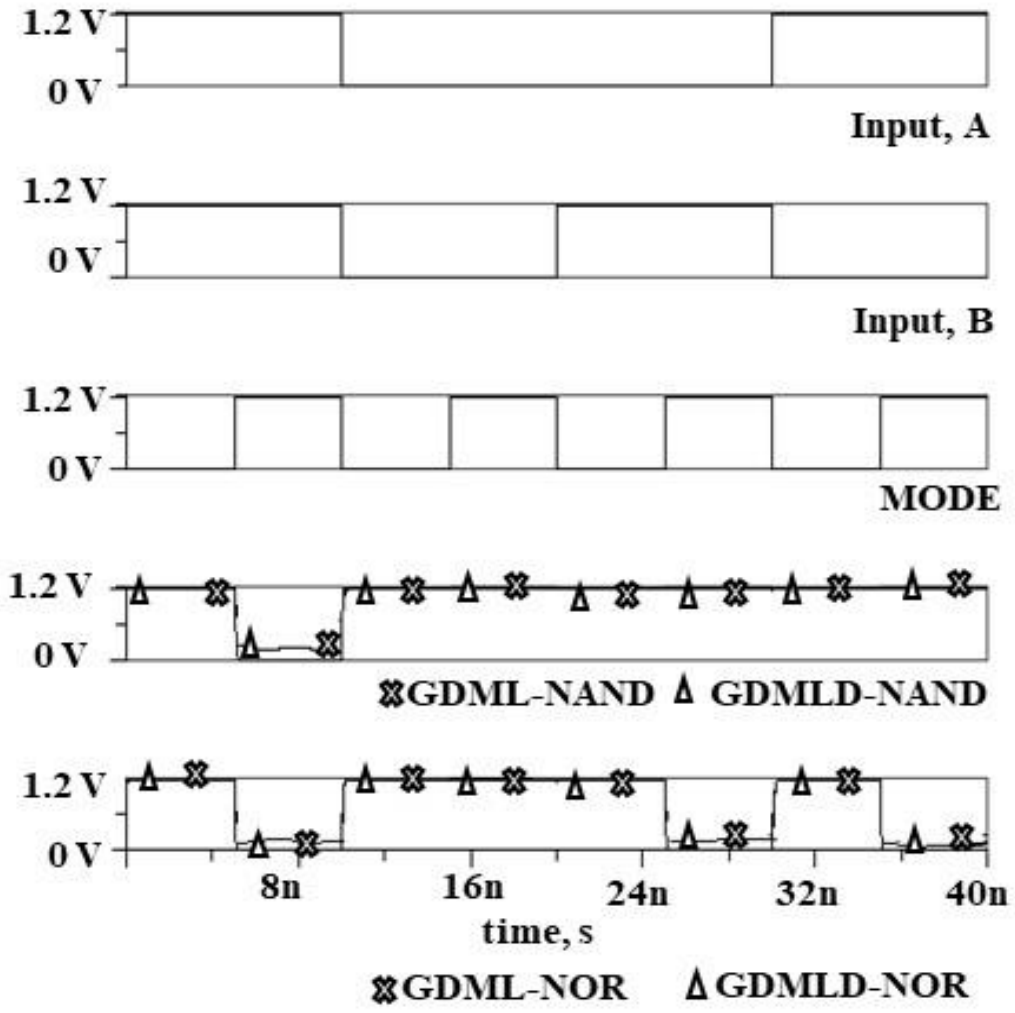



(b)

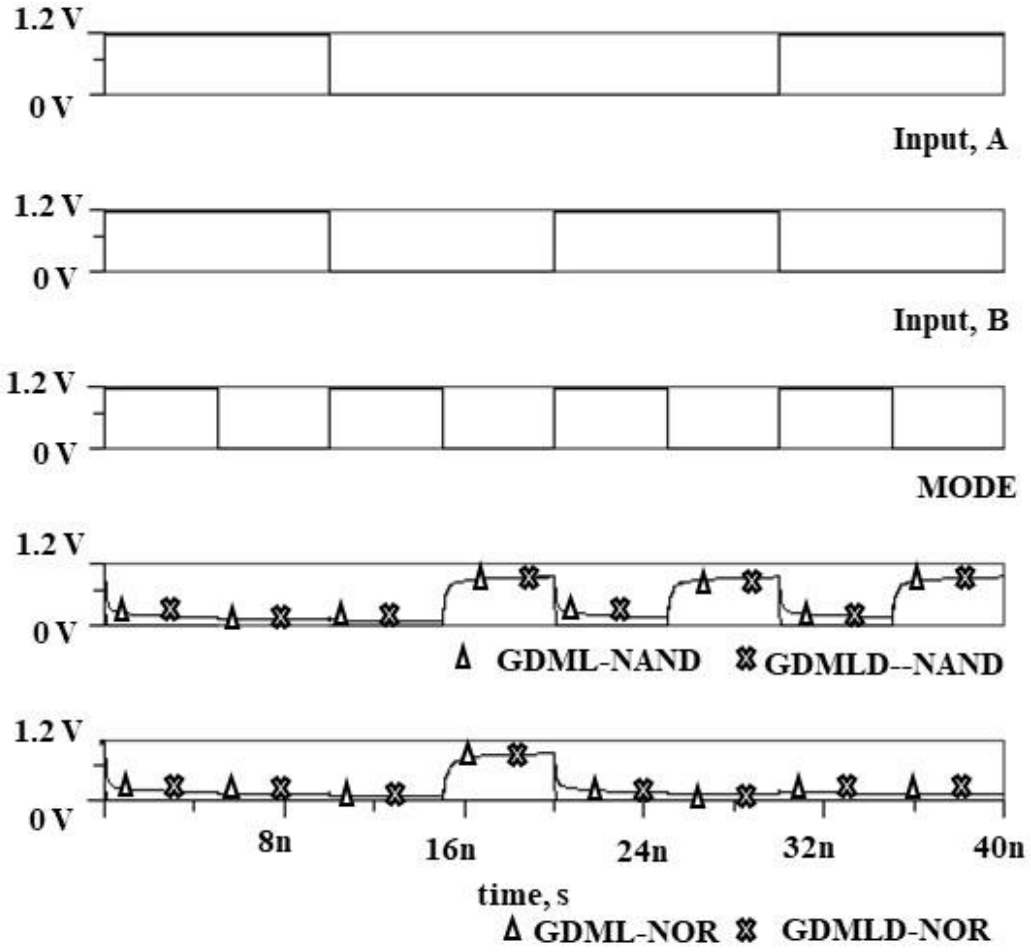
Fig. 3.17 Transient waveforms of the proposed GDML and GDMLD design in static mode (a) Type A NAND and NOR gate (b) Type B NAND and NOR gate

The dynamic mode of operation is depicted in Fig. 3.18. Here MODE input is connected to a clock signal having two phases of operation- pre-charge and evaluation. In pre-charge phase, MODE input is logic “0” for proposed type A gates, so the output is charged to supply voltage for both NAND and NOR gates. Alternatively, in evaluation phase, the MODE input becomes logic “1” for type A. Figure 3.18 (a) shows the transient waveform of the type A NAND and NOR gates in dynamic mode. It may be noted that in evaluation phase, output for NAND gate is logic “1” when any of the inputs is logic “0” whereas NOR gate provides output as logic “0” when any of the inputs is logic “1”. Thus, both the NAND and NOR gates based on GDML and GDMLD designs function correctly in dynamic mode.

The transient waveforms for type B NAND and NOR gates based on GDML and GDMLD designs in dynamic mode are illustrated in Fig. 3.18 (b). Here, the only difference is that for pre-discharge phase, the MODE input is logic “1” which discharges the output node to ground and for evaluation phase, the MODE input is logic “0”. In evaluation phase, the output for NAND gate is logic “1” when any of the inputs is logic “0” whereas NOR gate provides output logic “0” when any of the inputs is logic “1”.




(a)

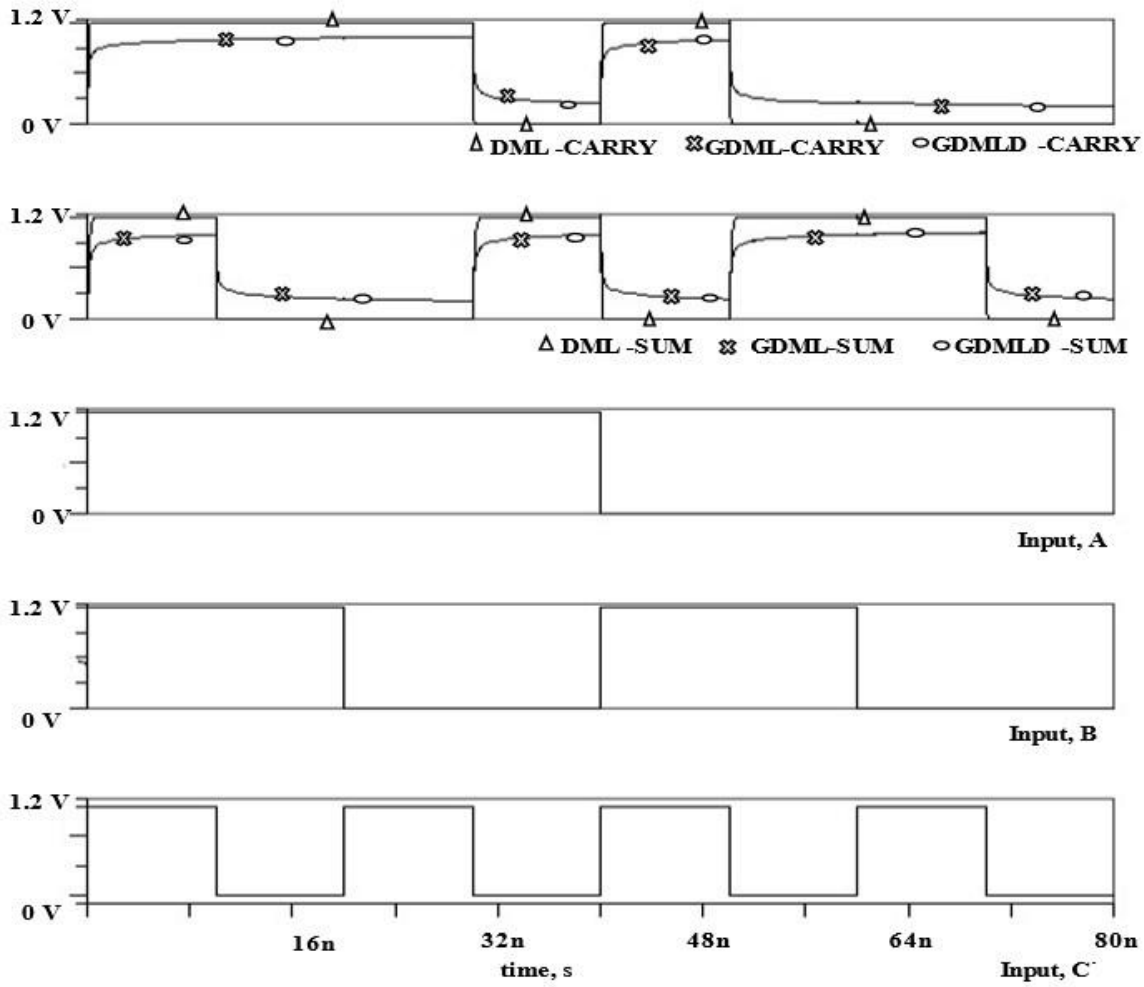



(b)

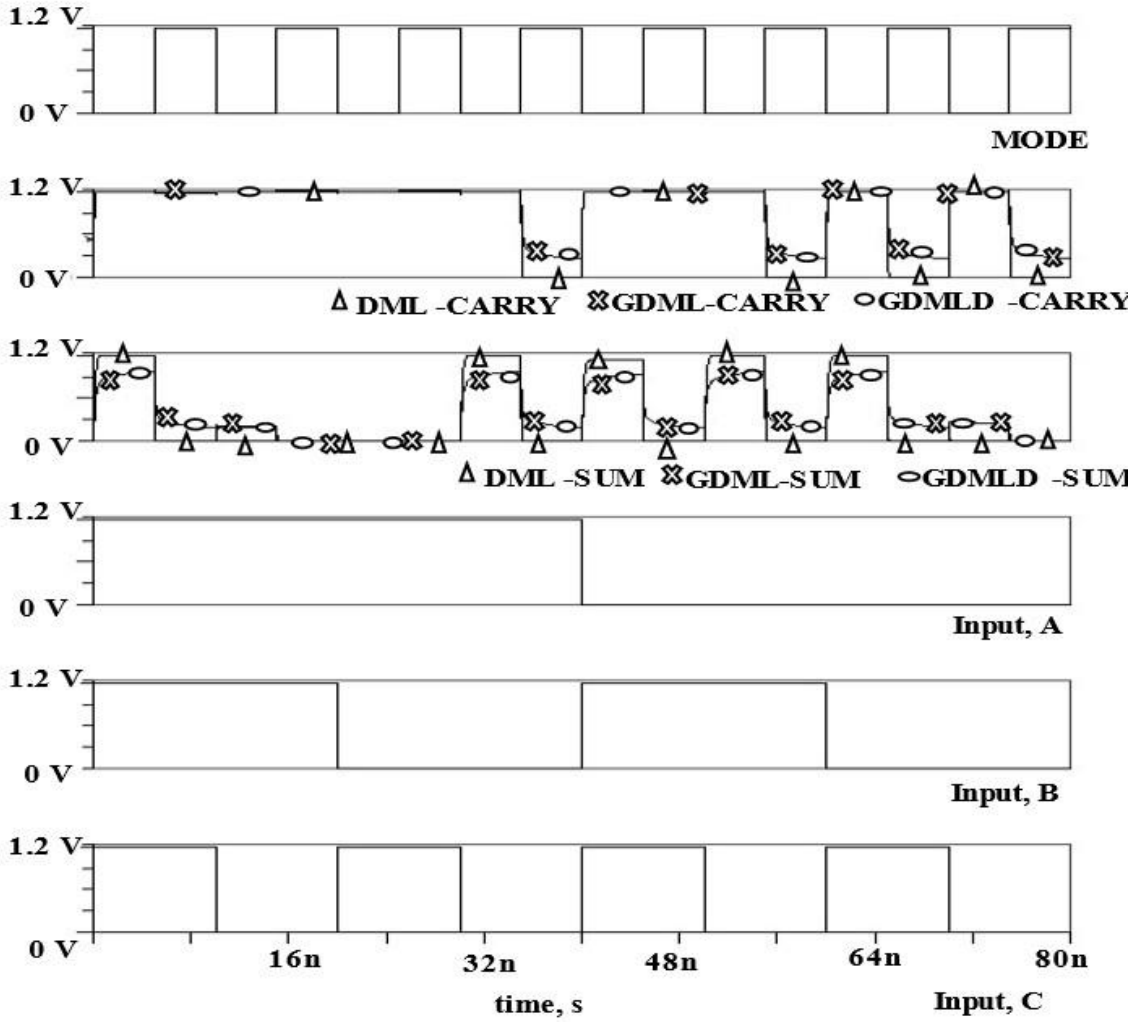
Fig. 3.18 Transient waveforms of the proposed GDML and GDMLD design in dynamic mode (a) Type A NAND and NOR gate (b) Type B NAND and NOR gate

Further, in order to show the cascading of type A and type B topologies of proposed GDML and GDMLD designs, a 1-bit FA circuit is also implemented using the schematic shown in Fig. 3.5. This schematic is realized using footed DML and proposed GDML and GDMLD designs. The sum block is implemented using type B topology and the carry block is implemented using type A topology. The functional verification of the FA is carried out by applying inputs A, B, C and MODE input as shown in Fig. 3.19. The transient waveforms for sum and carry for DML (DML-SUM, DML-CARRY), GDML (GDML-SUM, GDML-CARRY) and GDMLD (GDMLD-SUM, GDMLD-CARRY) are

depicted in Fig. 3.19 (a) and Fig. 3.19 (b) for static and dynamic mode respectively. It may be noted that in static mode, the SUM bit is logic “1” when an odd number of logic “1” among the inputs and the CARRY bit is logic “1” when at least two of the three inputs are logic “1”. In pre-charge/pre-discharge phase of dynamic mode, since the sum block is type B, therefore MODE is logic “1” causing the SUM bit to be at logic “0”. Similarly, since the carry block is type A therefore MODE is logic “0” as a result the CARRY bit is logic “1”. During the evaluation phase, the SUM bit becomes logic “1” when there's an odd number of logic “1” inputs, while the CARRY bit is logic “1” if at least two out of the three inputs are logic “1”.




(a)




(b)

Fig. 3.19 Transient waveforms of proposed GDML and GDMLD based 1-bit FA (a) Static mode (b) Dynamic mode

### 3.4.2.2 Performance comparison

The existing footed DML and proposed GDML and GDMLD designs are compared in static and dynamic mode in terms of leakage power, delay and leakage PDP for 2-input type A and type B NAND and NOR gates along with 1-bit FA circuit using Symica DE tool at 1.2 V supply voltage. Table 3.7 enlists the leakage power, delay and leakage PDP of the existing and the proposed 2-input type A and type B NAND and NOR gates and

1-bit FA in static mode at 90nm and 45nm respectively. Following are the observations from Table 3.7:

i. In static mode, the maximum leakage power saving is 51.95% for GDML and 77.96% for GDMLD at 90nm.

ii. The corresponding values are 74.11% for GDML and 90.08% for GDMLD at 45nm, i.e., the percentage leakage power saving increases with technology scaling.

iii. GDMLD variant has largest delay while GDML variants show a maximum increase of 25% in delay with respect to corresponding footed DML variants.

iv. Though the leakage PDP is more for GDMLD design, the leakage minimization is prime concern in battery operated devices as it drains battery when the device is in idle state.

v. With technology scaling, leakage power increases in static mode.

Table 3.7 Leakage power, delay and leakage PDP of proposed GDML, GDMLD and footed DML based 2-input type A and type B NAND and NOR gates, 1-bit FA circuit in static mode at 90nm and 45nm at 27°C

| | Circuit | Leakage Power(nW) | | | Delay(ns) | | | Leakage PDP(aJ) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 90nm | | Footed DML | GDML | GDMLD | Footed DML | GDML | GDMLD | Footed DML | GDML | GDMLD |
| | TA-NAND2 | 25.6 | 12.3 | 6.82 | 0.07 | 0.09 | 0.64 | 1.79 | 1.11 | 4.36 |
| | TB-NAND2 | 39.42 | 21.8 | 8.69 | 0.09 | 0.11 | 0.63 | 3.55 | 2.4 | 5.47 |
| | TA-NOR2 | 34.45 | 17.38 | 11.32 | 0.09 | 0.12 | 0.67 | 3.1 | 2.09 | 7.58 |
| | TB-NOR2 | 26.57 | 13.26 | 6.22 | 0.11 | 0.14 | 0.67 | 2.92 | 1.86 | 4.16 |
| | FA | 244.95 | 178.99 | 135.72 | 0.23 | 0.29 | 1.6 | 56.34 | 51.91 | 217.16 |
| 45nm | | | | | | | | | | |
| | TA-NAND2 | 133.91 | 34.67 | 13.8 | 0.05 | 0.07 | 0.36 | 6.7 | 2.43 | 4.97 |
| | TB-NAND2 | 205.21 | 73.27 | 38.96 | 0.07 | 0.09 | 0.33 | 14.36 | 6.59 | 12.86 |
| | TA-NOR2 | 184.91 | 51.32 | 25.04 | 0.07 | 0.09 | 0.33 | 12.94 | 4.62 | 8.26 |
| | TB-NOR2 | 135.93 | 39.88 | 13.48 | 0.08 | 0.11 | 0.32 | 10.87 | 4.39 | 4.31 |
| | FA | 974.49 | 412.15 | 345.12 | 0.09 | 0.15 | 0.84 | 87.7 | 61.82 | 517.68 |

The power, delay and leakage PDP of the existing and the proposed 2-input footed type A and type B DML NAND and NOR gates and 1-bit FA in dynamic mode (pre-charge and evaluation phase) at 90nm and 45nm is enlisted in Table 3.8. Following are the observations from Table 3.8:

i. During the pre-charge/ pre-discharge phase, GDML design results in a maximum percentage leakage power saving of 22.59% at 90nm, and 44.57% at 45nm.
ii. The GDMLD design results in a maximum percentage leakage power saving of 65.99% at 90nm, and 77.5% at 45nm in pre-charge/ pre-discharge phase.
iii. During the evaluation phase, GDML design results in a maximum percentage leakage power saving of 51.95% at 90nm, and 74.11% at 45nm.
iv. The GDMLD design results in a maximum percentage leakage power saving of 77.96% at 90nm, and 90.08% at 45nm in evaluation phase.
v. Both GDML and GDMLD variant show increase in delay as compared to corresponding footed DML variants in dynamic mode.
vi. The leakage power increases as technology is scaled from 90nm to 45nm in dynamic mode.
vii. With technology scaling, the efficacy of proposed designs increases at saving leakage power in dynamic mode.

Table 3.8 Leakage power, delay and leakage PDP of proposed GDML, GDMLD and footed DML based 2-input type A NAND and NOR gates, 2-input type B NAND and NOR gates, 1-bit FA in dynamic mode at 90nm and 45nm at 27°C

| | Circuit | Leakage Power(nW) | | | Delay(ns) | | | Leakage PDP(aJ) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 90nm | | Footed DML | GDML | GDMLD | Footed DML | GDML | GDMLD | Footed DML | GDML | GDMLD |
| Pre-charge/ Pre-discharge | TA-NAND2 | 5.88 | 4.92 | 2.45 | 0.03 | 0.07 | 0.67 | 0.18 | 0.34 | 1.64 |
| | TB-NAND2 | 10.12 | 9.06 | 7.79 | 0.05 | 0.08 | 0.45 | 0.51 | 0.72 | 3.5 |
| | TA-NOR2 | 16.38 | 12.73 | 5.57 | 0.02 | 0.07 | 0.52 | 0.33 | 0.89 | 2.9 |
| | TB-NOR2 | 3.36 | 3.18 | 2.87 | 0.06 | 0.08 | 0.51 | 0.2 | 0.25 | 1.46 |
| | FA | 51.34 | 39.74 | 35.74 | 0.11 | 0.14 | 1.35 | 5.65 | 5.56 | 48.25 |
| Evaluation | TA-NAND2 | 25.6 | 12.3 | 6.82 | 0.03 | 0.07 | 0.67 | 0.77 | 0.86 | 4.57 |
| | TB-NAND2 | 39.42 | 21.8 | 8.69 | 0.05 | 0.08 | 0.45 | 1.97 | 1.74 | 3.91 |
| | TA-NOR2 | 34.45 | 17.38 | 11.32 | 0.02 | 0.07 | 0.52 | 0.69 | 1.22 | 5.88 |
| | TB-NOR2 | 26.57 | 13.26 | 6.22 | 0.06 | 0.08 | 0.51 | 1.59 | 1.06 | 3.17 |
| | FA | 244.95 | 178.99 | 135.72 | 0.11 | 0.14 | 1.35 | 26.94 | 25.06 | 183.23 |
| 45nm | | | | | | | | | | |
| Pre-charge/ Pre-discharge | TA-NAND2 | 20.34 | 16.15 | 6.13 | 0.02 | 0.04 | 0.29 | 0.41 | 0.65 | 1.78 |
| | TB-NAND2 | 32.25 | 28.15 | 21.22 | 0.03 | 0.05 | 0.28 | 0.97 | 1.41 | 5.94 |
| | TA-NOR2 | 61.79 | 44.35 | 13.9 | 0.01 | 0.03 | 0.26 | 0.62 | 1.33 | 3.61 |
| | TB-NOR2 | 8.96 | 8.45 | 7.1 | 0.04 | 0.06 | 0.27 | 0.36 | 0.51 | 1.92 |
| | FA | 188.81 | 104.65 | 78.91 | 0.05 | 0.07 | 0.7 | 9.44 | 7.33 | 55.24 |
| Evaluation | TA-NAND2 | 133.91 | 34.67 | 13.8 | 0.02 | 0.04 | 0.29 | 2.68 | 1.39 | 4 |
| | TB-NAND2 | 205.21 | 73.27 | 38.96 | 0.03 | 0.05 | 0.28 | 6.16 | 3.66 | 5.31 |
| | TA-NOR2 | 184.91 | 51.32 | 25.04 | 0.01 | 0.03 | 0.26 | 1.85 | 1.54 | 6.51 |
| | TB-NOR2 | 135.93 | 39.88 | 13.48 | 0.04 | 0.06 | 0.27 | 5.44 | 2.39 | 3.64 |
| | FA | 974.49 | 698.15 | 545.12 | 0.05 | 0.07 | 0.7 | 48.72 | 48.87 | 381.58 |

Further, the efficiency of the proposed design in terms of percentage leakage power saving is investigated at different temperatures i.e., -25 °C, 27 °C and 100 °C at 90nm and 45nm in static and dynamic mode. In static mode, the percentage leakage power saving achieved using proposed designs for 2-input type A and type B NAND and NOR gates,

1-bit FA circuit for -25 °C, 27 °C and 100 °C at 90nm and 45nm is enlisted in Tables 3.9 and 3.10 respectively. Following are the observations from Tables 3.9 and 3.10:

i. There is a decrease in leakage power in footed DML designs with the incorporation of proposed GDML and GDMLD design across different temperature in static mode.

ii. Percentage leakage power saving obtained varies from 30.48% to 80.9% and 61.48% to 92.67% for 90nm and 45nm respectively at -25℃.

iii. The range of percentage leakage power saving in proposed designs is 26.93% to 77.96% for 90nm and 57.71% to 90.09% for 45nm at 27℃.

iv. The percentage leakage power saving is 22.78% to 72.22% for 90nm and by 53.58% to 85.81% for 45nm at 100℃.

Table 3.9 Percentage leakage power saving for 2-input type A and type B NAND and NOR gates, 1-bit FA in static mode for different temperature at 90nm

| 90nm Process Technology, $V_{DD}$ =1.2 V, Static Mode of DML | | | | | | |
|---|---|---|---|---|---|---|
| Circuit | Percentage leakage power saving at -25℃ | | Percentage leakage power saving at 27℃ | | Percentage leakage power saving at 100℃ | |
| | GDML | GDMLD | GDML | GDMLD | GDML | GDMLD |
| TA-NAND2 | 56.12 | 75.25 | 51.96 | 73.38 | 48.15 | 68.48 |
| TB-NAND2 | 47.44 | 80.9 | 44.69 | 77.96 | 40.57 | 72.22 |
| TA-NOR2 | 53.9 | 72.12 | 49.56 | 67.15 | 44.88 | 63.31 |
| TB-NOR2 | 54.59 | 79.92 | 50.09 | 76.6 | 45.59 | 71.38 |
| FA | 30.48 | 49.12 | 26.93 | 44.59 | 22.78 | 41.71 |

Table 3.10 Percentage leakage power saving for 2-input type A and type B NAND and NOR gates, 1-bit FA circuit in static mode for different temperature at 45nm

| 45nm Process Technology, $V_{DD}$ =1.2 V, Static Mode of DML | | | | | | |
|---|---|---|---|---|---|---|
| Circuit | Percentage leakage power saving at -25℃ | | Percentage leakage power saving at 27℃ | | Percentage leakage power saving at 100℃ | |
| | GDML | GDMLD | GDML | GDMLD | GDML | GDMLD |
| TA-NAND2 | 76.44 | 92.67 | 74.11 | 89.69 | 70.89 | 84.41 |
| TB-NAND2 | 67.78 | 84.76 | 64.29 | 81.01 | 59.9 | 77.89 |
| TA-NOR2 | 75.62 | 89.91 | 72.24 | 86.46 | 68.91 | 81.33 |
| TB-NOR2 | 73.22 | 92.12 | 70.66 | 90.09 | 65.56 | 85.81 |
| FA | 61.48 | 67.79 | 57.71 | 64.58 | 53.58 | 60.11 |

In dynamic mode, the percentage leakage power saving achieved for 2-input type A and type B NAND and NOR gates, 1-bit FA circuit for -25 °C, 27 °C and 100 °C at 90nm and 45nm is enlisted in Tables 3.11 and 3.12 respectively. Following are the observations from Tables 3.11 and 3.12:

i. There is a decrease in leakage power in proposed GDML and GDMLD as compared to footed DML design across different temperature in dynamic mode

ii. At -25℃, percentage leakage power saving is 9.28% to 80.9% for 90nm and 11.99% to 92.67% for 45nm in dynamic mode.

iii. At 27℃, percentage leakage power saving is 5.36% to 77.96% for 90nm and 5.69% to 90.09% for 45nm in dynamic mode.

iv. At 100℃, percentage leakage power saving is 4.77% to 72.22% for 90nm and 5.1% to 85.81% for 45nm in dynamic mode.

Table 3.11 Percentage leakage power saving for 2-input type A and type B NAND and NOR gates, 1-bit FA circuit in dynamic mode for different temperature at 90nm

| 90nm Process Technology, $V_{DD}$ =1.2 V, Dynamic Mode of DML | | | | | | |
|---|---|---|---|---|---|---|
| | Percentage leakage power saving at -25℃ | | Percentage leakage power saving at 27℃ | | Percentage leakage power saving at 100℃ | |
| Pre-charge/ Pre-discharge | GDML | GDMLD | GDML | GDMLD | GDML | GDMLD |
| TA-NAND2 | 20.15 | 61.78 | 16.28 | 58.34 | 9.65 | 53.97 |
| TB-NAND2 | 13.34 | 27.61 | 10.5 | 23.07 | 9.1 | 20.18 |
| TA-NOR2 | 25.57 | 69.87 | 22.27 | 66.01 | 18.52 | 63.11 |
| TB-NOR2 | 9.28 | 23.02 | 5.36 | 14.64 | 4.77 | 14.1 |
| FA | 26.44 | 33.9 | 22.58 | 30.38 | 18.8 | 25.69 |
| Evaluation | | | | | | |
| TA-NAND2 | 56.12 | 75.25 | 51.96 | 73.38 | 48.15 | 68.48 |
| TB-NAND2 | 47.44 | 80.9 | 44.69 | 77.96 | 40.57 | 72.22 |
| TA-NOR2 | 53.9 | 72.12 | 49.56 | 67.15 | 44.88 | 63.31 |
| TB-NOR2 | 54.59 | 79.92 | 50.09 | 76.6 | 45.59 | 71.38 |
| FA | 30.48 | 49.12 | 26.93 | 44.59 | 22.78 | 41.71 |

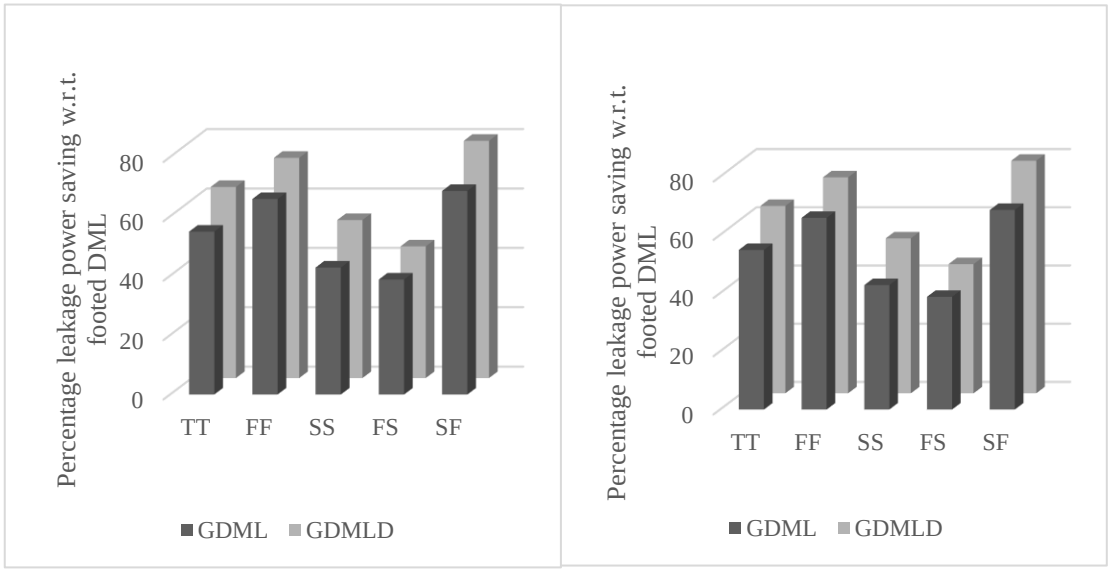
Table 3.12 Percentage leakage power saving for 2-input type A and type B NAND and NOR gates, 1-bit FA circuit in dynamic mode for different temperature at 45nm

| 45nm Process Technology, $V_{DD}$ =1.2 V, Dynamic Mode of DML | | | | | | |
|---|---|---|---|---|---|---|
| | Percentage leakage power saving at -25℃ | | Percentage leakage power saving at 27℃ | | Percentage leakage power saving at 100℃ | |
| Pre-charge/ Pre-discharge | GDML | GDMLD | GDML | GDMLD | GDML | GDMLD |
| TA-NAND2 | 28.99 | 75.66 | 20.6 | 69.86 | 16.75 | 65.11 |
| TB-NAND2 | 19.52 | 40.38 | 12.69 | 34.2 | 10.89 | 30.58 |
| TA-NOR2 | 35.05 | 88.5 | 28.22 | 77.51 | 22.88 | 71.48 |
| TB-NOR2 | 11.99 | 24.52 | 5.69 | 20.69 | 5.1 | 18.43 |
| FA | 49.8 | 64.45 | 44.57 | 58.21 | 33.9 | 47.17 |
| Evaluation | | | | | | |
| TA-NAND2 | 76.44 | 92.67 | 74.11 | 89.69 | 70.89 | 84.41 |
| TB-NAND2 | 67.78 | 84.76 | 64.29 | 81.01 | 59.9 | 77.89 |
| TA-NOR2 | 75.62 | 89.91 | 72.24 | 86.46 | 68.91 | 81.33 |
| TB-NOR2 | 73.22 | 92.12 | 70.66 | 90.09 | 65.56 | 85.81 |
| FA | 61.48 | 67.79 | 57.71 | 64.58 | 53.58 | 60.11 |

Additionally, the robustness of the proposed GDML and GDMLD design is checked by considering a 2-input type A NAND gate and analysing it at five different process corners i.e., TT, FF, SS, FS, SF. The percentage leakage power saving for the proposed GDML and GDMLD based 2-input type A NAND gate compared to the existing footed DML counterpart across five distinct process corners in static mode, pre-charge phase of dynamic mode, and evaluation phase of dynamic mode is depicted in Fig. 3.20, Fig. 3.21 and Fig. 3.22, respectively.

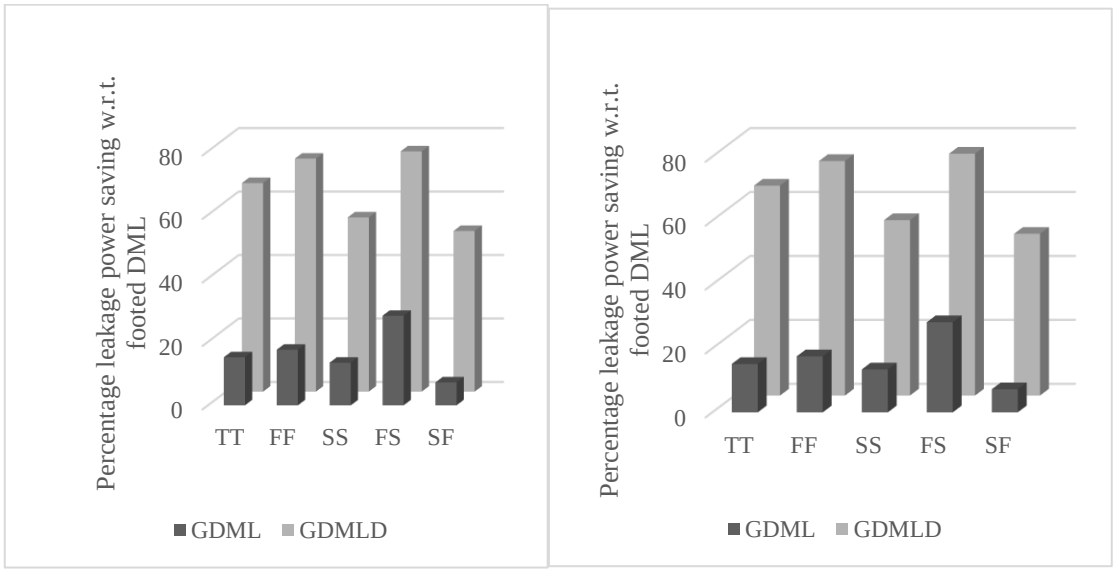
In static mode, GDML demonstrates a maximum percentage leakage power saving of 68.55%, while GDMLD showcases an even greater saving of 79.9% for both 90nm and 45nm technologies. Correspondingly, during the pre-charge phase of dynamic mode, the values stand at 28.19% for GDML and 75.66% for GDMLD. During the evaluation phase, GDML exhibits a 68.55% percentage leakage power saving, whereas GDMLD shows an even higher saving of 79.9% for both 90nm and 45nm. These results suggest that the proposed design-II effectively has less leakage power when compared to

the existing footed DML design across all process corners in both static and dynamic mode.



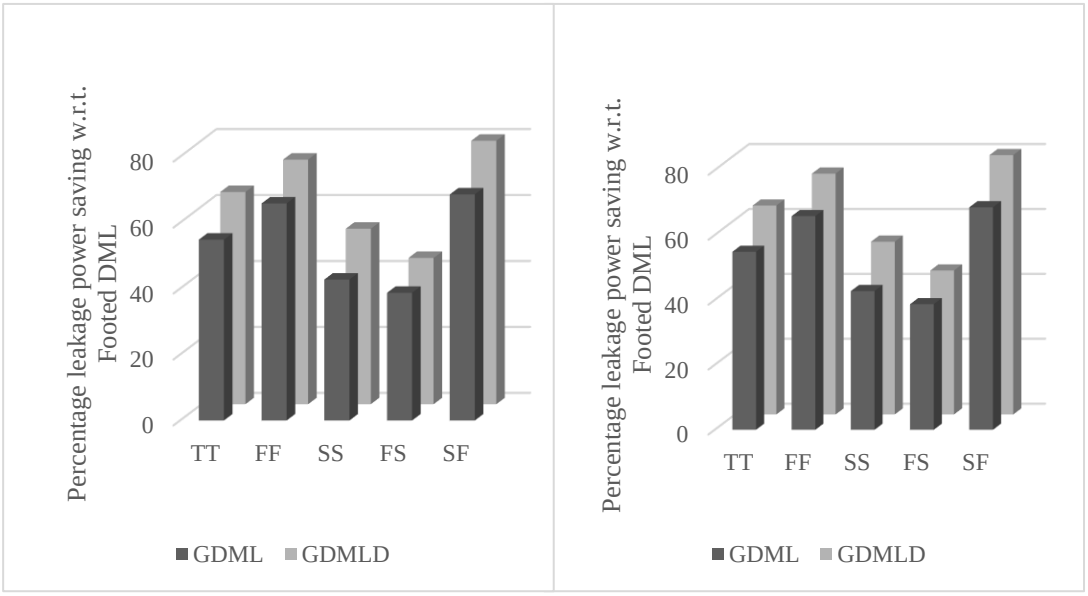

(a) (b)

Fig. 3.20 Percentage leakage power saving for proposed GDML and GDMLD based 2-input type A NAND gate at five different process corners in static mode at (a) 90nm (b) 45nm




(a) (b)

Fig. 3.21 Percentage leakage power saving for proposed GDML and GDMLD based 2-input type A NAND gate at five different process corners in pre-charge phase of dynamic mode at (a) 90nm (b) 45nm

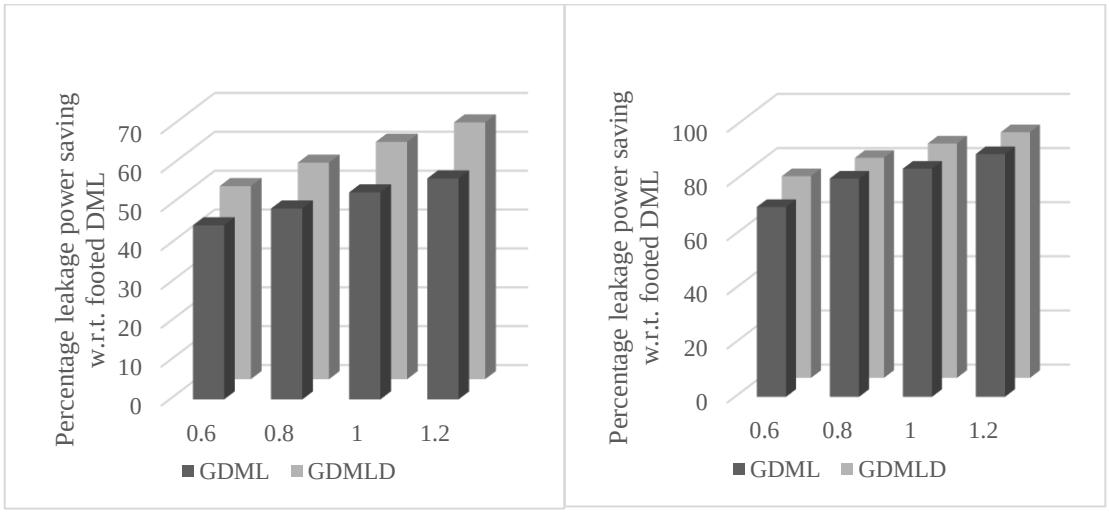



(a) (b)

Fig. 3.22 Percentage leakage power saving for proposed GDML and GDMLD based 2-input type A NAND gate at five different process corners in evaluation phase of dynamic mode at (a) 90nm (b) 45nm

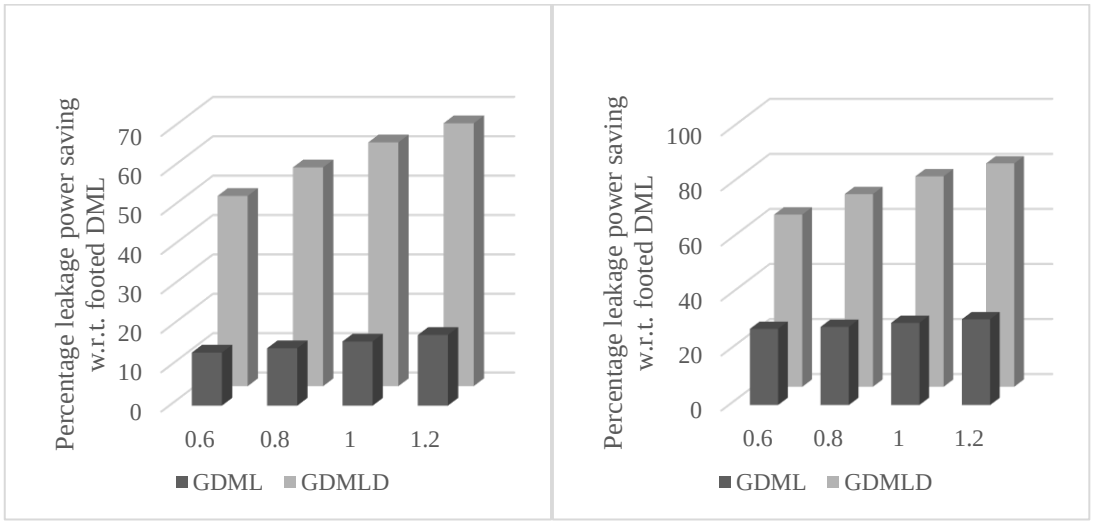
The effectiveness of the proposed design is further examined by using the proposed GDML and GDMLD based 2-input type A NAND gate across various supply voltages (ranging from 0.6 V to 1.2 V) at both 90nm and 45nm. Figure 3.23, Figure 3.24 and Figure 3.25 depict the percentage leakage power saving attained using GDML and GDMLD designs in the static mode, pre-charge phase of dynamic mode, and evaluation phase of dynamic mode, respectively. Notably, proposed design-II proves efficient in terms of leakage power saving across all supply voltages in both static and dynamic mode, demonstrating maximum percentage leakage power saving of 56.83% and 66.04% at 90nm and 89.68% and 90.76% at 45nm for GDML and GDMLD designs, respectively, in static mode. Similarly, in the pre-charge phase of dynamic mode, the corresponding savings stand at 17.94% and 66.76% at 90nm and 31.16% and 81.78% at 45nm for GDML and GDMLD design, respectively. During the evaluation phase, the maximum percentage

leakage power saving reaches 56.83% and 66.04% at 90nm and 89.68% and 90.76% at 45nm for GDML and GDMLD design, respectively.



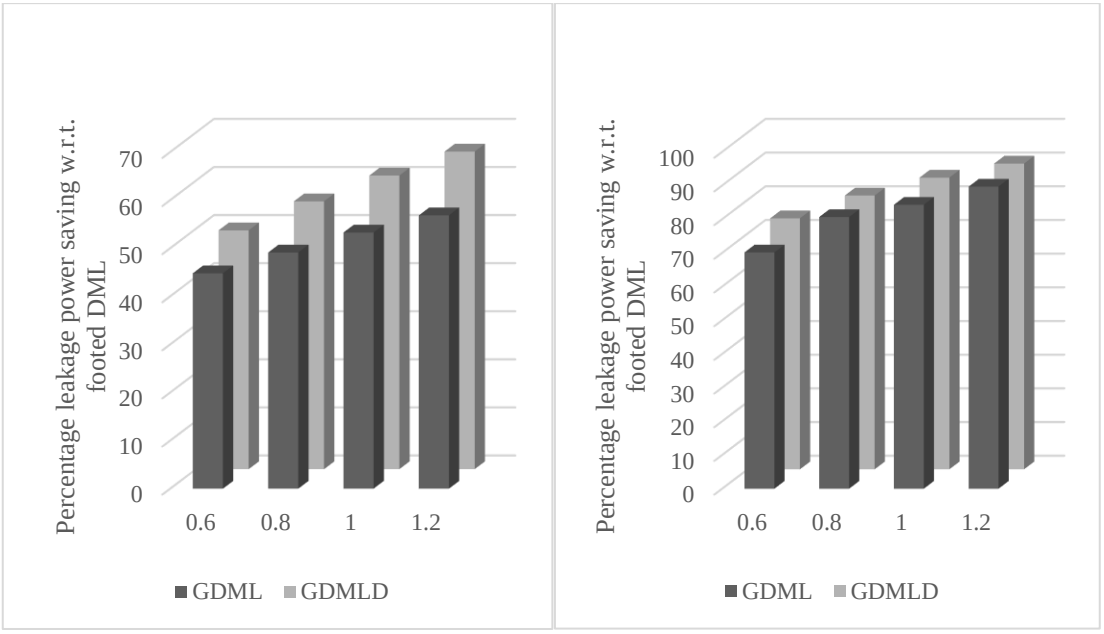

(a) (b)

Fig. 3.23 Percentage leakage power saving for proposed GDML and GDMLD based 2-input type A NAND gate at different voltages in static mode at (a) 90nm (b) 45nm




(a) (b)

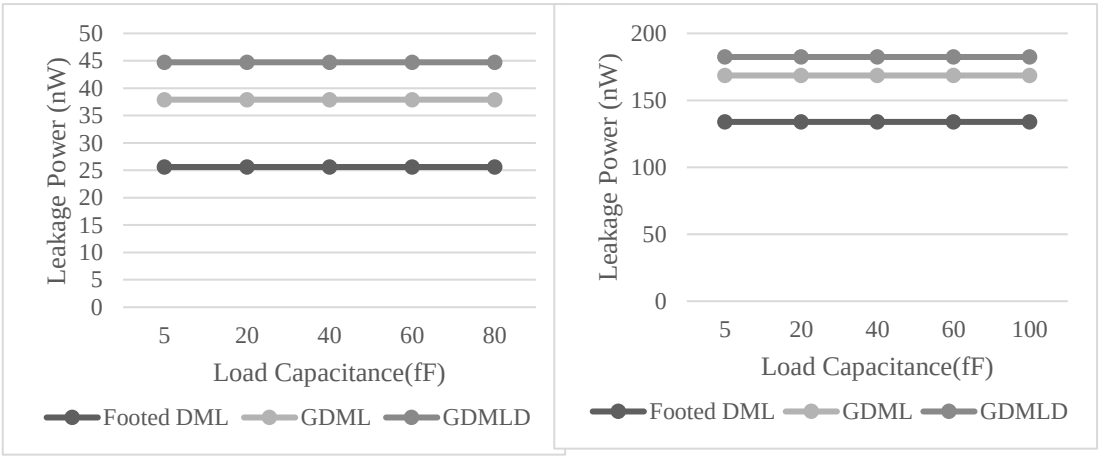
Fig. 3.24 Percentage leakage power saving for proposed GDML and GDMLD based 2-input type A NAND gate at different voltages in pre-charge phase of dynamic mode at (a) 90nm (b) 45nm




(a) (b)

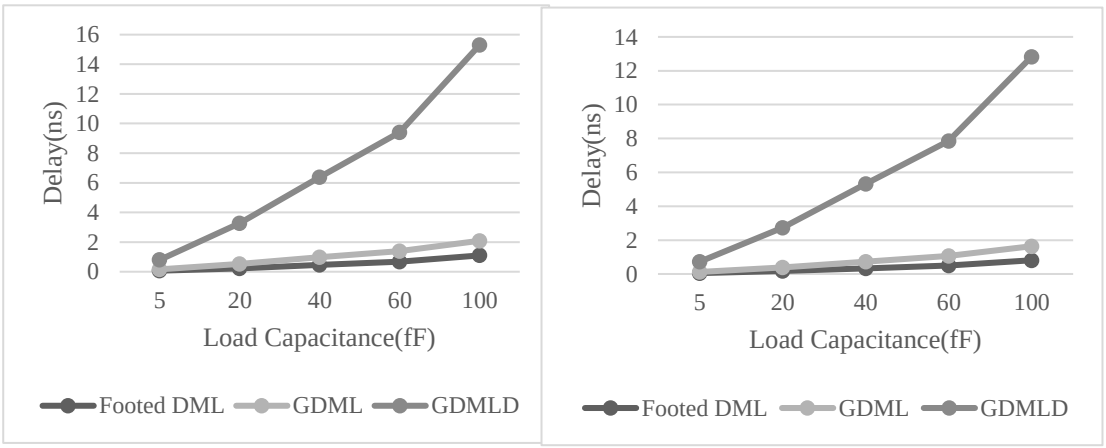
Fig. 3.25 Percentage leakage power saving for proposed GDML and GDMLD based 2-input type A NAND gate at different voltages in evaluation phase of dynamic mode at (a) 90nm (b) 45nm

Further, the variation in leakage power and delay is also observed for 2-input type A NAND gate by varying load capacitor (5fF-100fF) at 90nm and 45nm as depicted in Fig. 3.26 and 3.27, respectively. It may be observed that with increase in load capacitance value, the leakage power remains constant. However, there is an increase in delay value with increase in load capacitance and the effect is more severe in case of GDMLD design compared to GDML design.




(a) (b)

Fig. 3.26 Effect of variation of load capacitance on leakage power for footed DML, proposed GDML and GDMLD based 2-input type A NAND gate (a) 90nm (b) 45nm




(a) (b)

Fig. 3.27 Effect of variation of load capacitance on delay for footed DML, proposed GDML and GDMLD based 2-input type A NAND gate (a) 90nm (b) 45nm

A summary of observations based on the data enlisted in Tables 3.7-3.12 is as follows:

i. There is a surge in the leakage power of the existing and proposed design with technology scaling i.e., from 90nm to 45nm.

ii. The proposed GDML and GDMLD designs show better performance in terms of leakage power saving at lower technology node i.e., the percentage leakage power saving is enhanced at 45nm as compared with that of 90nm.

iii. The GDMLD design proves to be more efficient at leakage power saving in all circuits than the GDML design.

iv. The reason behind better GDMLD performance in terms of percentage leakage power saving is mainly due to the presence of footed diode transistor which provides more stacking effect.

v. Delay of the DML design increase due to incorporation of GLTs in the proposed designs. The increase is more for GDMLD design as compared to the GDML design.

vi. For a 1-bit FA, significant percentage leakage power saving is witnessed using the proposed GDML and GDMLD designs. The proposed GDMLD design is more effective in combating leakage power as compared to GDML design.

## 3.5 Conclusion

In this chapter, LDML, GDML, and GDMLD designs are proposed by incorporating LECTOR and GALEOR leakage reduction techniques into footed DML design. Proposed design-I uses LCT transistors with standard and high VTH to combat leakage, while proposed design-II employs GLT transistors with or without a footed diode transistor. Extensive simulations are conducted to compare these designs in terms of leakage power, delay, and leakage PDP, while also analysing the effects of temperature variation, technology scaling, supply voltage variation and load capacitance variation. In static mode, LDML achieves a maximum leakage power saving of 30.49% at 90nm, increasing to 57.32% at 45nm, while LDML-HIGH-VTH reaches 44.85% at 90nm and 66.61% at 45nm. During the pre-charge/pre-discharge phase, LDML provides savings of

17.22% at 90nm and 34.99% at 45nm, while LDML-HIGH-VTH improves to 29.98% at 90nm and 40.42% at 45nm. In dynamic mode, during the evaluation phase, LDML achieves 30.49% leakage savings at 90nm and 57.32% at 45nm, whereas LDML-HIGH-VTH provides the highest savings of 44.85% at 90nm and 66.61% at 45nm. In static mode, GDML achieves a maximum leakage power saving of 68.55%, while GDMLD reaches 79.9% for both 90nm and 45nm nodes, indicating higher efficiency. During the pre-charge phase in dynamic mode, GDML provides a 28.19% leakage power saving, whereas GDMLD achieves a significantly higher 75.66% savings. In the evaluation phase, GDML again maintains a 68.55% saving, while GDMLD demonstrates the highest leakage power saving at 79.9% for both technology nodes. All the simulation results are pre-layout, however there may be a variation of 10-15% for post layout results. Corner analysis is also performed to check the robustness of the proposed designs. The simulations show that LDML with high VTH LCTs is more efficient at reducing leakage than the LDML design with standard VTH, but it results in increased delay. Meanwhile, GDMLD is more effective at leakage power saving than GDML, but it also causes more delay. With technology scaling, the efficacy of the proposed designs improves, although the leakage power increases. The proposed LDML,GDML and GDMLD are efficient at leakage power saving across different temperature, voltage and process corners. The leakage power remains constant with variation in load capacitance however, increase in load capacitance causes an increase in delay, with GDMLD having the most significant effect. The comparative analysis shows that while GDML and GDMLD design are more efficient at leakage power saving, LDML design has better leakage PDP due to lower delay.

# Chapter 4

# Modified DMTGDI and Dual Mode DCVSL Design

The contents of this chapter are published in:

[1] N. Yadav, N. Pandey, and D. Nand, **"Modified Dual Mode Transmission Gate Diffusion Input logic for improving energy efficiency,"** J. Circuits Syst. Comput., 2022, doi: 10.1142/S0218126623501712. (SCIE indexing, 1.5 IF)

[2] N. Yadav, N. Pandey and D. Nand, **"Energy Efficient Dual Mode DCVSL (DM-DCVSL) design,"** 2023 Second International Conference on Electrical, Electronics, Information and Communication Technologies (ICEEICT), Trichirappalli, India, 2023, pp. 01-05, doi: 10.1109/ICEEICT56924.2023.10157481.

## 4.1 Introduction

The impact of incorporating leakage reduction techniques, namely LECTOR and GALEOR, in footed DML design is analyzed in Chapter 3. The CMOS structure of footed DML design is replaced with pre-existing logic styles that can act as an alternative to CMOS. Two alternatives are worked upon, namely DMTGDI and DCVSL, in this chapter.

In type A and type B DMTGDI designs presented in Chapter 2, it is found that certain input combinations can lead to contention during the pre-charge/pre-discharge phase due to the presence of a path between the supply voltage and ground. To alleviate this issue, Modified Dual Mode TGDI (M-DMTGDI) is proposed in this chapter. Further, dual mode capability is introduced in DCVSL and such design is termed as Dual Mode DCVSL (DM-DCVSL). It uses additional transistors to support both static and dynamic mode of operation. This design combines the strengths of both DML and DCVSL in a unified design.

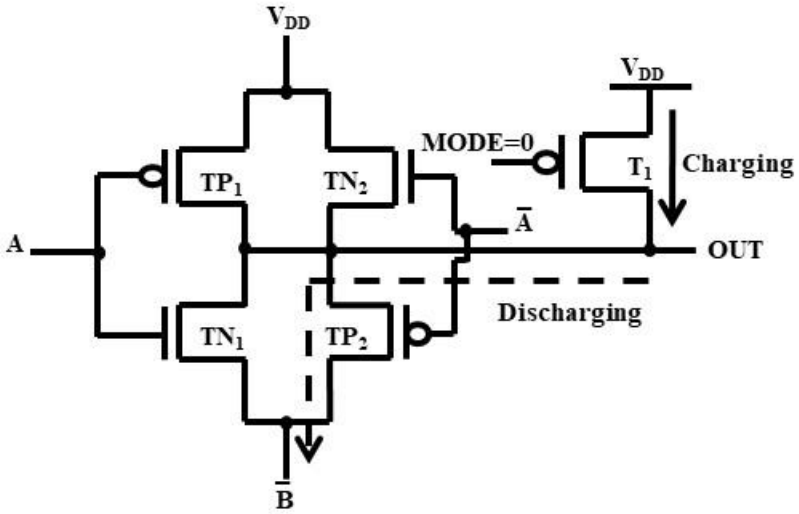
## 4.2 Proposed Design-III: M-DMTGDI

This section first discusses the issue of contention in pre-charge phase of DMTGDI design. To elucidate this, a DMTGDI based 2-input NAND gate (Fig. 4.1 (a)) is considered. In pre-charge phase operation of the circuit, MODE is logic "0" which makes transistor $T_1$ on. Now for both inputs (A, B) as logic "1", transistors $TN_1$ and $TP_2$ are on, so a path is established between $V_{DD}$ and ground. It restricts the output voltage to reach up to $V_{DD}$ and violates the condition of dynamic gate i.e. output pre-charged to $V_{DD}$.

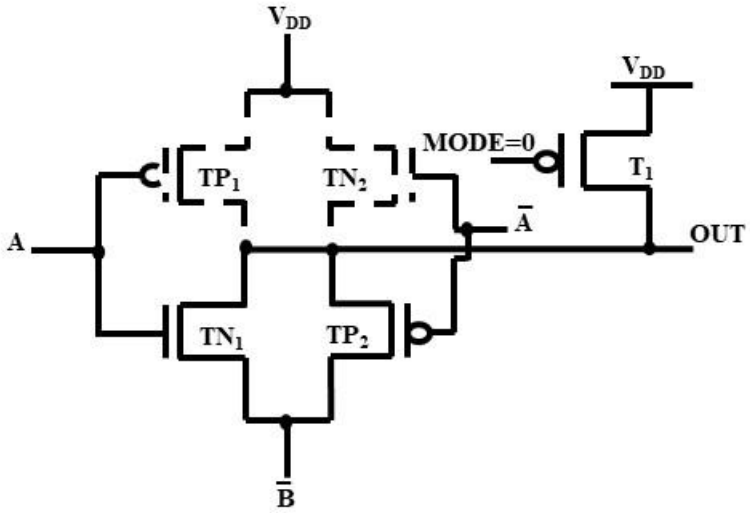
To find the output in such case, the circuit of Fig. 4.1 (a) is redrawn as Fig. 4.1 (b), where 'on' transistors are represented with solid lines and 'off' transistors with dotted

lines. The output of this circuit may be obtained by identifying the region of operation of transistors $T_1$, $TN_1$ and $TP_2$ and solving KCL at output node.

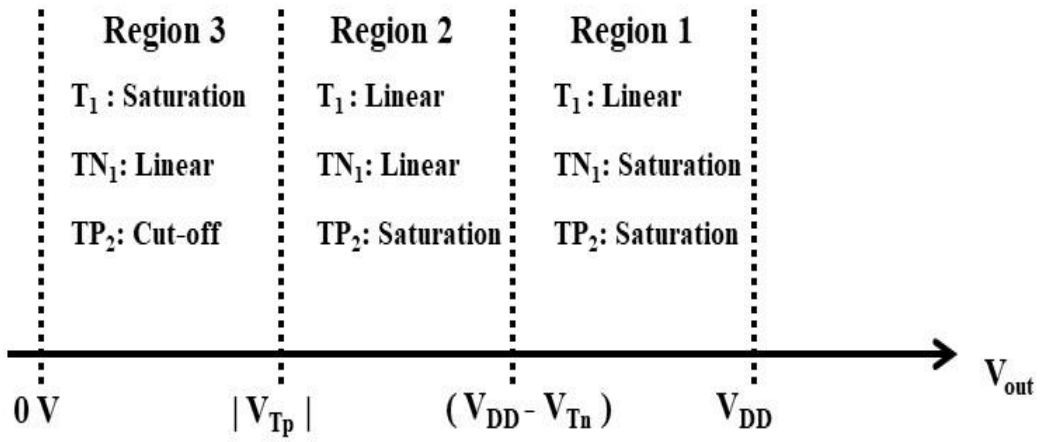
Assuming the output node is at $V_{DD}$ prior to switching operation in dynamic mode. Consequently, on applying a logic "0" on MODE input and applying both inputs (A, B) as logic "1", the output voltage starts reducing. The operating region of transistors $T_1$, $TN_1$ and $TP_2$ depends on output voltage, which is shown in Fig. 4.1 (c).




(a)




(b)




(c)

Fig. 4.1 (a) DMTGDI based 2-input NAND gate in pre-charge phase of dynamic mode for (A, B) = (1,1) (b) Equivalent circuit of (a) (c) Bias conditions and operating regions of the DMTGDI based 2-input NAND gate

The exact value of the output may be obtained by solving appropriate KCL equations in region I, region II and region III, considering $I_{D,T1}$, $I_{D,TN1}$ and $I_{D,TP2}$ as drain currents for transistors $T_1$, $TN_1$ and $TP_2$ respectively. The other symbols used have their usual meaning. Table 4.1 enlists the region of operation of transistors $T_1$, $TN_1$ and $TP_2$ under different operating conditions.

Table 4.1 Region of operation of transistors $T_1$, $TN_1$ and $TP_2$

| Transistor | $V_{out} < \|V_{Tp}\|$ | $\|V_{Tp}\| < V_{out} < V_{DD} - V_{Tn}$ | $V_{out} >= V_{DD} - V_{Tn}$ |
|---|---|---|---|
| $T_1$ | Saturation | Linear | Linear |
| $TN_1$ | Linear | Linear | Saturation |
| $TP_2$ | Cut-off | Saturation | Saturation |

Region I: For $V_{out} \geq V_{DD} - V_{Tn}$ , the transistor $T_1$ remains in linear region while $TN_1$ and $TP_2$ operate in saturation region, as shown in Fig. 4.1 (c). Therefore, a KCL at output node gives

$$I_{D,T1}\,(\text{linear}) = I_{D,TN1}(\text{sat}) + I_{D,TP2}(\text{sat}) \tag{4.1 a}$$

$$\mu_p C_{ox}\left(\frac{W}{L}\right)_{T1} [\, 2\,(-V_{DD} - V_{Tp})\,(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\,]$$

$$= \mu_n C_{ox}\left(\frac{W}{L}\right)_{TN1} (V_{DD} - V_{Tn})^2 + \mu_p C_{ox}\left(\frac{W}{L}\right)_{TP2} (-V_{out} - V_{Tp})^2 \tag{4.1 b}$$

Region II: For $|V_{TP}| < V_{out} < V_{DD} - V_{Tn}$, the transistor $T_1$ and $TN_1$ remain in linear region while $TP_2$ operate in saturation region, as shown in Fig. 4.1 (c). Therefore, a KCL at output node gives

$$I_{D,T1}(\text{linear}) = I_{D,TN1}(\text{linear}) + I_{D,TP2}(\text{sat}) \tag{4.2 a}$$

$$\mu_p C_{ox}\left(\frac{W}{L}\right)_{T1} [\, 2\,(-V_{DD} - V_{Tp})\,(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\,]$$

$$= \mu_n C_{ox}\left(\frac{W}{L}\right)_{TN1} [\, 2\,(V_{DD} - V_{Tn})\,(V_{out}) - V^2_{out})\,] + \mu_p C_{ox}\left(\frac{W}{L}\right)_{TP2} (-V_{out} - V_{Tp})^2 \tag{4.2 b}$$

Region III: For $V_{out} < |V_{TP}|$, the transistor $T_1$ enters in saturation region while $TN_1$ remains in linear region and $TP_2$ turns off, as shown in Fig. 4.1 (c). Therefore, a KCL at output node gives

$$I_{D,T1}(\text{sat}) = I_{D,TN1}(\text{linear}) + I_{D,TP2}(\text{cut-off}) \tag{4.3 a}$$

$$\mu_p C_{ox}\left(\frac{W}{L}\right)_{T1} (-V_{DD} - V_{Tp})^2 = \mu_n C_{ox}\left(\frac{W}{L}\right)_{TN1} [\, 2\,(V_{DD} - V_{Tn})\,(V_{out}) - V^2_{out})\,] \tag{4.3 b}$$

To eliminate the contention issue of DMTGDI design in pre-charge phase of dynamic mode, the TGDI cell is used in conjunction with a footed DML inverter to

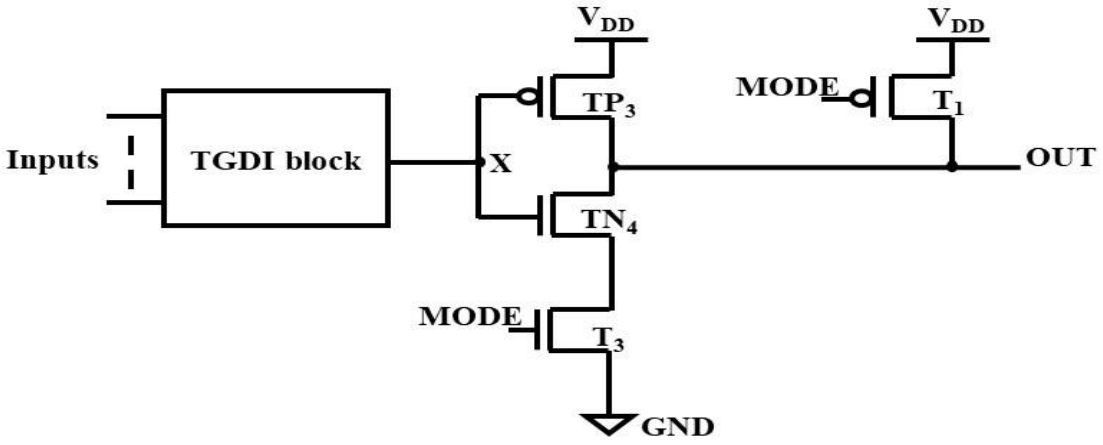
achieve dual mode operation, The cell so derived is called Modified DMTGDI (M-DMTGDI) cell and is shown in Fig. 4.2.

### 4.2.1 Operation

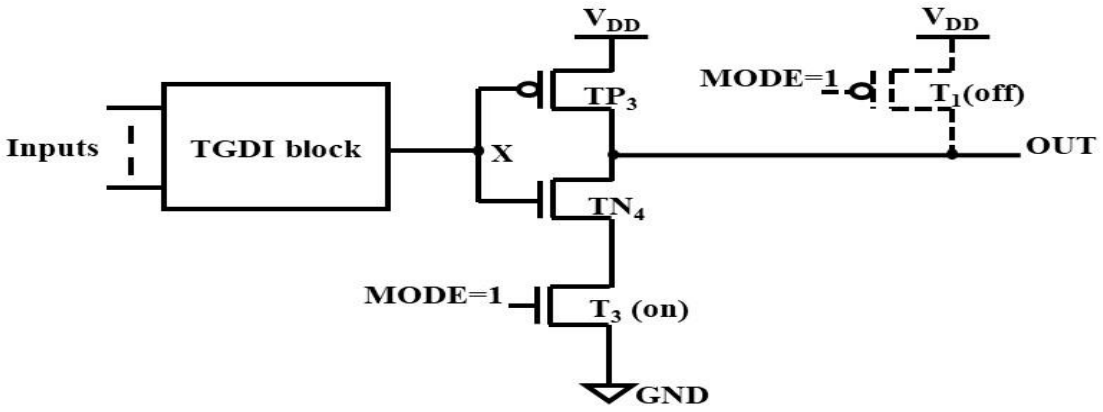
In this subsection, the operation of proposed M-DMTGDI design, shown in Fig. 4.2, is described in static and dynamic mode. For static mode, the MODE input is logic "1", making transistor $T_1$ off and the footer transistor $T_3$ on at the same time. The circuit is redrawn in Fig. 4.2 (b) where 'on' transistors are represented with solid lines and 'off' transistors with dotted lines. Thus, the output of the TGDI block is applied to a footed DML inverter and the final output will be complement of node X's voltage.

The dynamic mode of operation namely, pre-charge and evaluate, are elucidated in Fig. 4.2 (c) and 4.2 (d) respectively. In this case, MODE input is connected to clock. When clock is logic "0" (pre-charge phase), the transistor $T_1$ establishes a path between $V_{DD}$ and output node and pre-charges the output node to $V_{DD}$. It may be noted that the path from $V_{DD}$ to ground does not exist in this case as the footer transistor, $T_3$ is off.

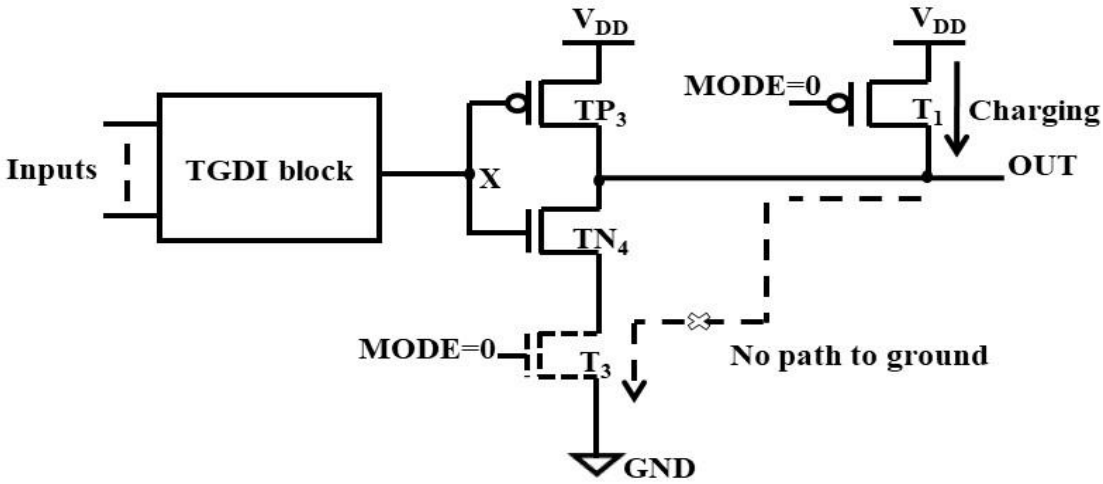
In evaluation phase, transistor $T_1$ is off and the footer transistor $T_3$ is on, the output is evaluated according to the inputs applied, as shown in Fig. 4.2 (d), where 'on' transistors are represented with solid lines and 'off' transistors with dotted lines.



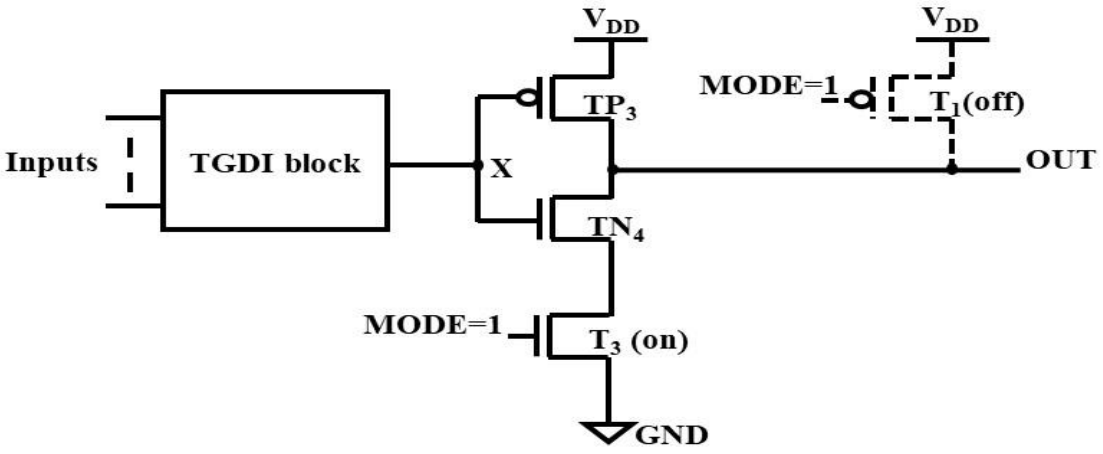

(a)




(b)



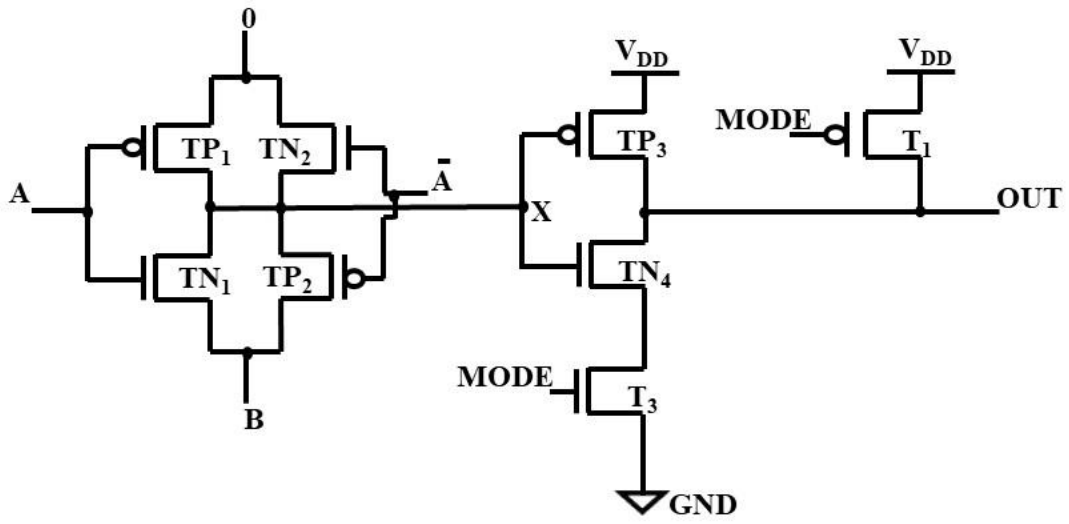

(c)



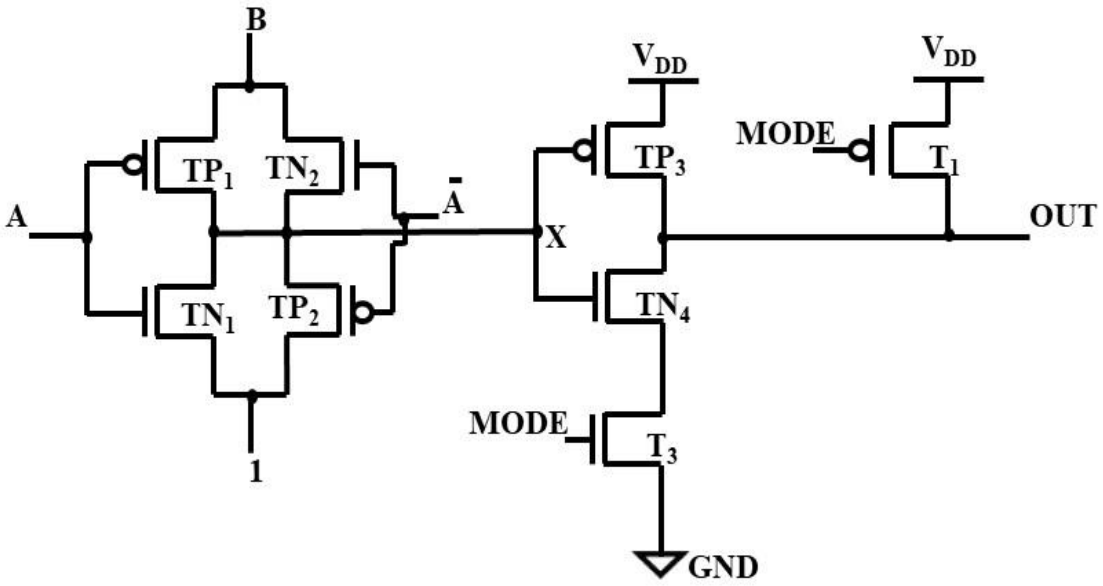

(d)

Fig. 4.2 (a) Proposed M-DMTGDI cell (b) Proposed M-DMTGDI cell in static mode (c) Proposed M-DMTGDI cell in pre-charge phase of dynamic mode (d) Proposed M-DMTGDI cell in evaluation phase of dynamic mode

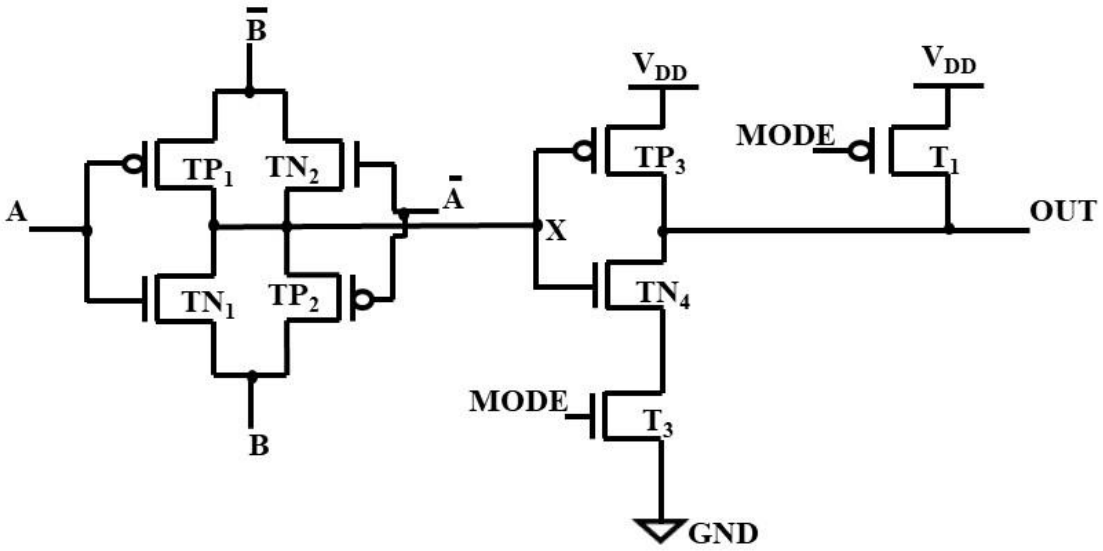
The TGDI block of proposed M-DMTGDI design can be reconfigured to implement 2-input NAND, NOR and XOR gates, which can be used to realize complex logic functions. The proposed M-DMTGDI based 2-input NAND, NOR and XOR gates are shown in Fig. 4.3.




(a)




(b)




(c)

Fig. 4.3 Proposed M-DMTGDI based gate (a) 2-input NAND gate (b) 2-input NOR gate (c) 2-input XOR gate

### 4.2.2 Simulation results

This section consists of two subsections namely functional verification to examine the working of the proposed M-DMTGDI design and performance comparison of the existing and proposed designs in terms of power, delay, and PDP. Footed DML, DMTGDI and proposed M-DMTGDI based designs are simulated using Symica DE tool for 2-input NAND, NOR and XOR gates using 90nm BSIM4 model card for bulk CMOS at 1.2 V supply voltage and load capacitance of 5fF. Further, a 1-bit FA circuit is also examined. Corner analysis is done for all the circuits both in static and dynamic mode. Effect of voltage and temperature variation is also investigated. The SPICE simulator SymSpice is used to demonstrate the operation of proposed designs. SymProbe tool is used for power and delay analysis.

#### 4.2.2.1 Functional verification

The 2-input gates- NAND, NOR and XOR gates, are designed using proposed M-DMTGDI design in static and dynamic mode. The transient waveforms for NAND,

NOR and XOR gates in static mode are shown in Fig. 4.4. It may be noted that output for NAND gate is logic "1" when any of the inputs is logic "0" whereas NOR gate provides output logic "0" when any of the inputs is logic "1". For XOR gate, the output is logic "1" when there is odd number of logic "1" inputs otherwise, the output is logic "0". Thus, proposed M-DMTGDI based NAND, NOR and XOR gate work correctly in static mode.

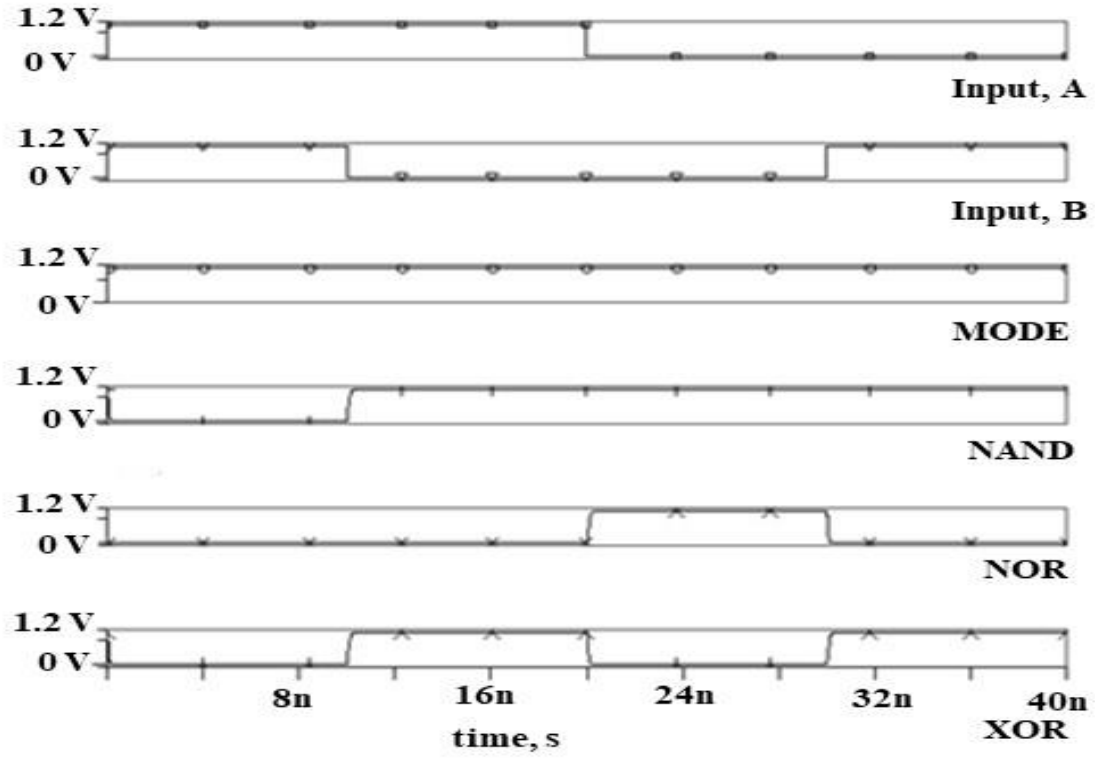



Fig. 4.4 Transient waveforms of proposed M-DMTGDI design for 2-input gates in static mode

Figure 4.5 depicts the transient waveforms of the proposed M-DMTGDI based 2-input NAND, NOR and XOR gates in dynamic mode. In pre-charge phase of dynamic mode (MODE=logic "0"), the output is charged to $V_{DD}$ irrespective of inputs applied for NAND, NOR and XOR gates. However, in evaluation phase (MODE= logic "1"), the output for NAND gate is logic "1" when any of the inputs is logic "0" whereas NOR gate provides output logic "0" when any of the inputs is logic "1". For XOR gate, the output

is logic “1” when there is odd number of logic “1” inputs otherwise, the output is logic “0”.

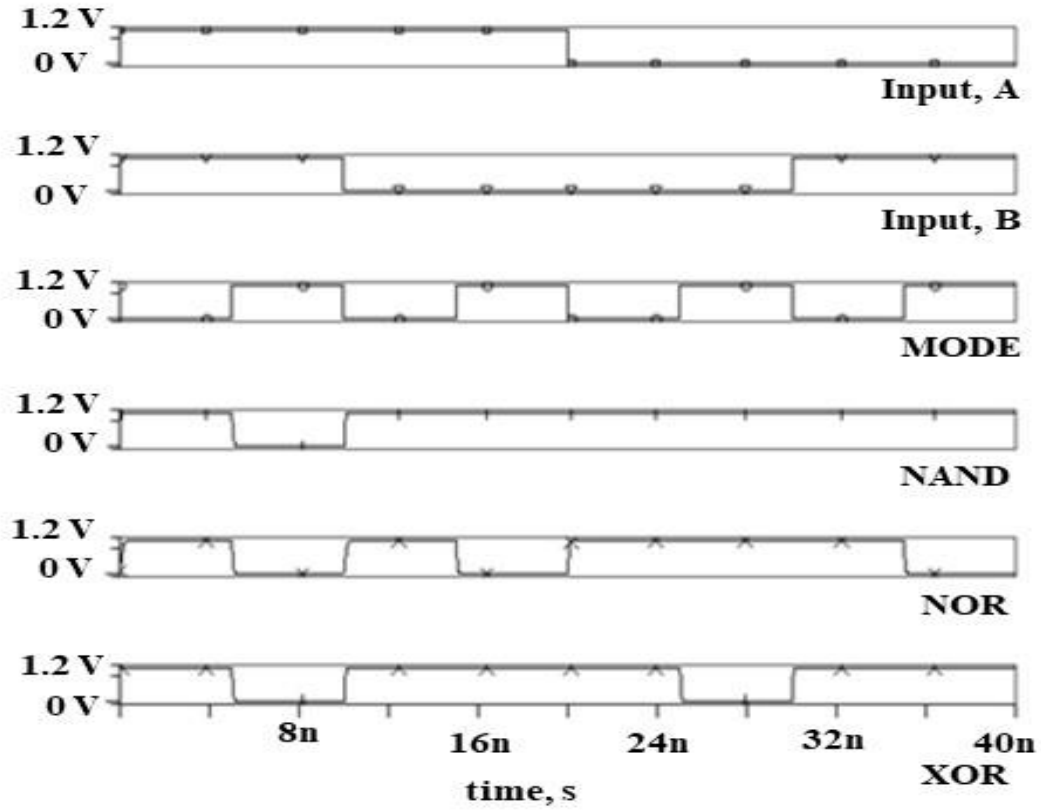
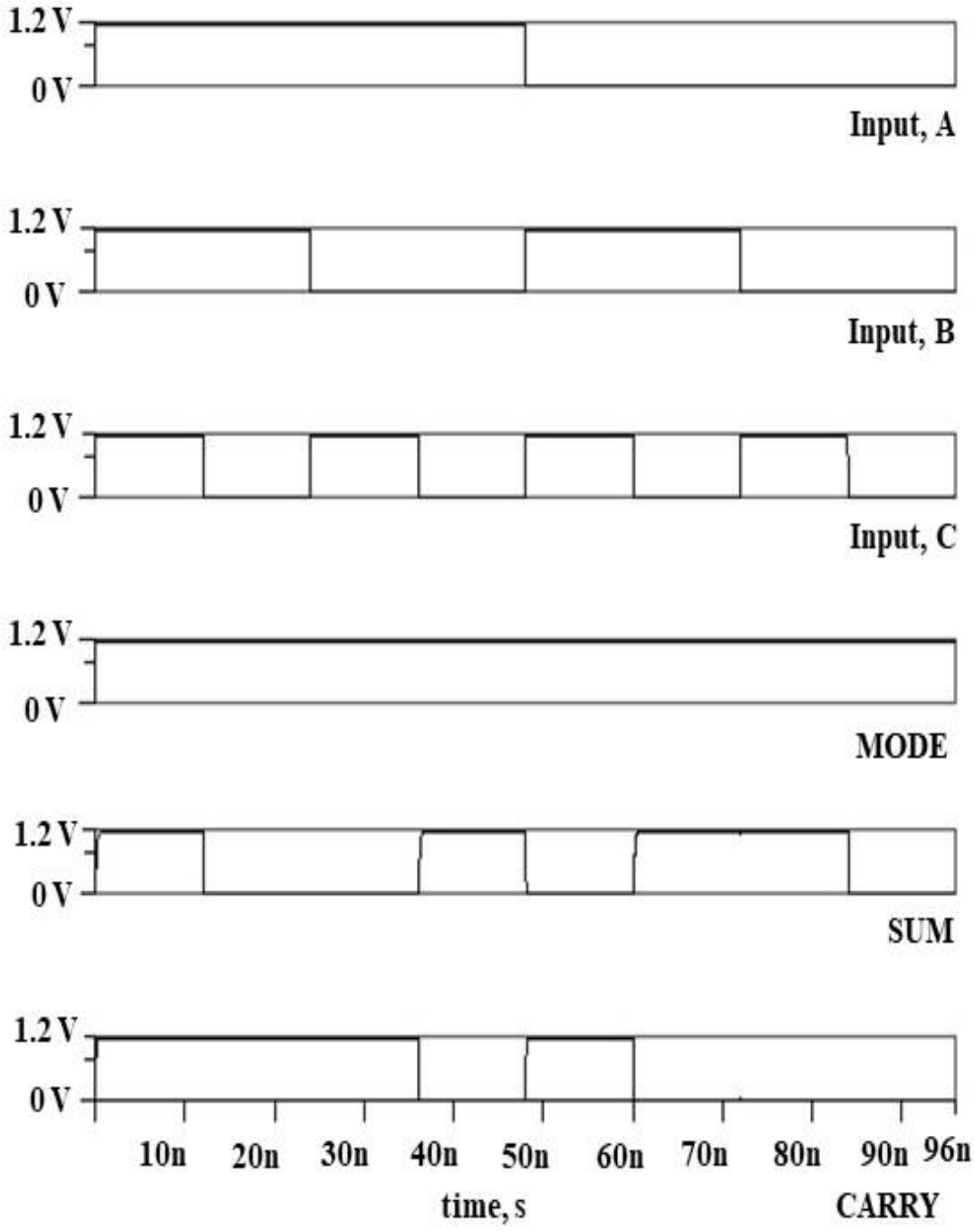


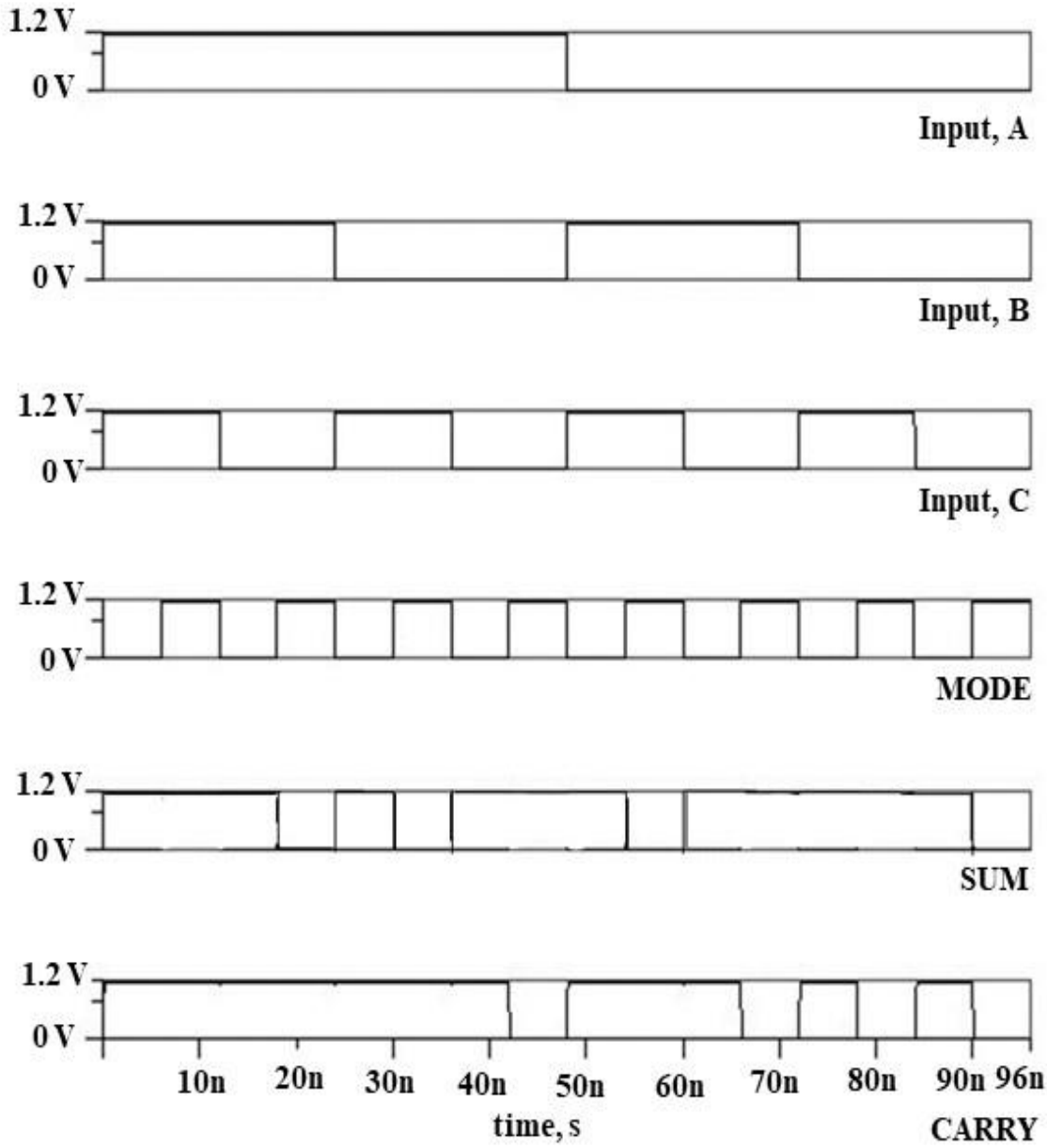

Fig. 4.5 Transient waveforms of proposed M-DMTGDI design for 2-input gates in dynamic mode

A 1-bit FA circuit is also implemented using the proposed M-DMTGDI design. The SUM block generates SUM bit which is generated by using two TGDI based XNOR gates, as given in Table 2.1, followed by a footed DML inverter. A two-stage network (CARRY block) is used to generate the CARRY bit where first stage consists of three TGDI based NAND gates and the second stage consists of a TGDI based AND gate, followed by a footed DML inverter The applied input waveforms for inputs A,B,C and MODE input (MODE) are depicted in Fig. 4.6. The transient waveforms for sum (SUM) and carry (CARRY) are depicted in Fig. 4.6 (a) and Fig. 4.6 (b) for static and dynamic mode respectively. It may be noted that in static mode, the SUM bit is logic “1” when an odd number of logic “1” among the inputs and the CARRY bit is logic “1” when at least

two of the three inputs are logic “1”. In pre-charge phase of dynamic mode, the SUM and CARRY bit are logic “1” as MODE input is logic “0”. During the evaluation phase, the SUM bit becomes logic “1” when there's an odd number of logic “1” inputs, while the CARRY bit is logic “1” if at least two out of the three inputs are logic




(a)




(b)

Fig. 4.6 Transient waveforms of proposed M-DMTGDI based 1-bit FA (a) Static mode (b) Dynamic mode

#### 4.2.2.2 Performance comparison

For comparison of performance of the existing designs and the proposed M-DMTGDI design in terms of power, delay and PDP, 2-input NAND, NOR, XOR gates and 1-bit FA circuit are considered. The simulations are performed using Symica DE tool at 1.2 V supply voltage and load capacitance of 5fF using 90nm BSIM4 model card for bulk CMOS. The power, delay and PDP of the existing and the proposed 2-input NAND,

NOR, XOR gates and 1-bit FA circuit in static and dynamic mode at 27℃ are enlisted in Table 4.2. Following observations are made from Table 4.2:

i. There is an increase in PDP of the proposed M-DMTGDI design as compared to its DMTGDI counterpart, but PDP is less than that of its footed DML counterpart in static mode.

ii. In dynamic mode, there is a significant improvement in PDP of the proposed design as compared to the existing footed DML and DMTGDI designs i.e., the proposed design has lowest PDP in dynamic mode.

iii. For 2-input gates, a maximum PDP reduction of 33.07% and 97.38% as compared to their footed DML and DMTGDI counterparts is achieved. For 1-bit FA circuit, the corresponding values are 87.19% and 99.79%.

iv. The DMTGDI based design shows increase in PDP values as compared to footed DML design in dynamic mode.

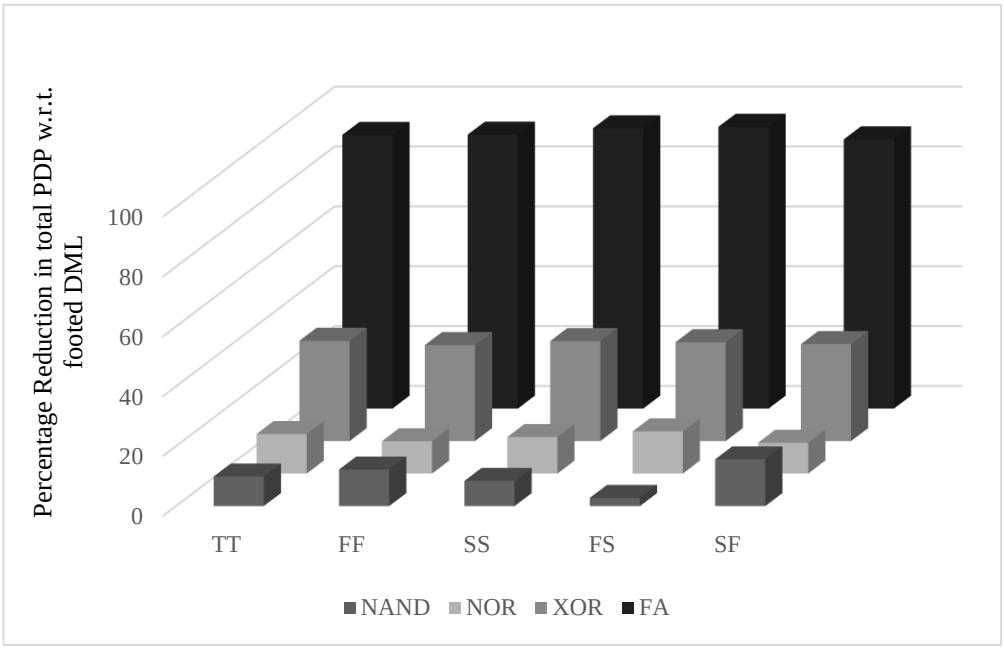
v. The reduction in PDP is notably higher when utilizing the proposed M-DMTGDI design in dynamic mode compared to static mode. Consequently, operating the proposed M-DMTGDI design in dynamic mode for over 50% longer duration than in static mode demonstrates significantly enhanced PDP efficiency compared to prolonged operation in static mode.

Table 4.2 Power, delay and PDP of proposed M-DMTGDI, DMTGDI and footed DML based 2-input NAND, NOR, XOR gates and 1-bit FA circuit in static and dynamic mode at 27°C

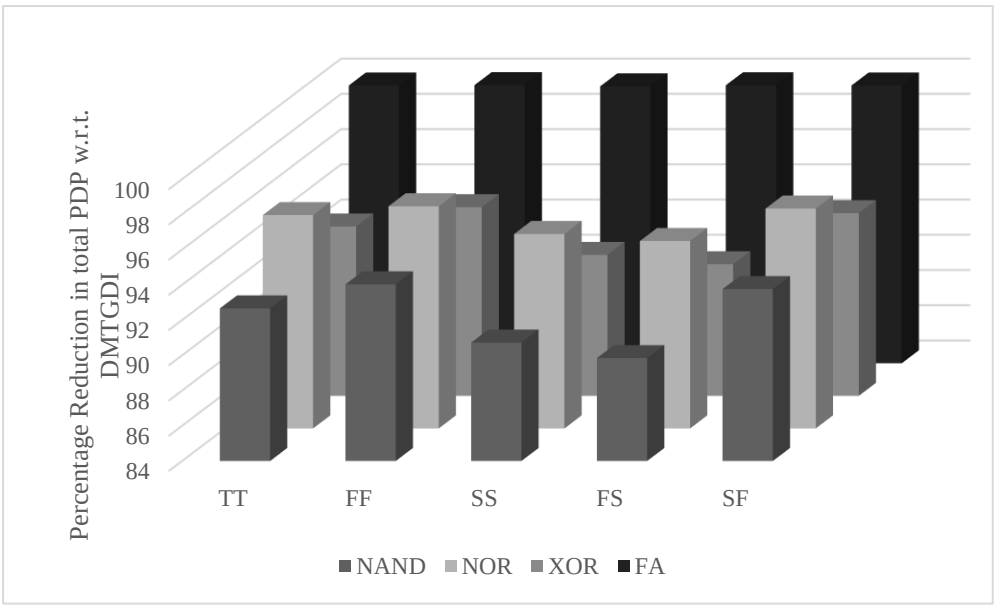
| Mode | Circuit | Power(uW) | | | Delay(ps) | | | PDP(aJ) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Footed DML | DMTGDI | M-DMTGDI | Footed DML | DMTGDI | M-DMTGDI | Footed DML | DMTGDI | M-DMTGDI |
| Static | NAND | 0.46 | 0.46 | 0.43 | 74.29 | 33.08 | 68.98 | 34.17 | 15.22 | 29.66 |
| | NOR | 0.44 | 0.04 | 0.44 | 94.36 | 33.28 | 68.15 | 41.52 | 1.33 | 29.99 |
| | XOR | 0.84 | 0.047 | 0.82 | 97.6 | 31.3 | 66.11 | 81.98 | 1.47 | 54.21 |
| | FA | 5.82 | 1.27 | 2.38 | 123.43 | 33.44 | 82.65 | 718.36 | 42.47 | 196.71 |
| Dynamic | | | | | | | | | | |
| | NAND | 0.94 | 85.18 | 0.89 | 35 | 8.16 | 25.28 | 32.9 | 695.07 | 22.5 |
| | NOR | 2.71 | 263.44 | 2.67 | 23.61 | 8.93 | 23.06 | 63.98 | 2352.52 | 61.57 |
| | XOR | 2 | 170.54 | 1.87 | 32.23 | 8.92 | 23.07 | 64.46 | 1521.22 | 43.14 |
| | FA | 15.46 | 2790 | 5.87 | 69.77 | 24.36 | 23.53 | 1078.64 | 67964.4 | 138.12 |

Further, to check the robustness of the proposed M-DMTGDI design, corner analysis is done for all circuits- 2-input NAND gate, 2-input NOR gate, 2-input XOR gate and 1-bit FA at five different process corners i.e., TT, FF, SS, FS, SF. The percentage reduction in total PDP in both static and dynamic mode for proposed 2-input NAND, NOR, XOR gates and 1-bit FA circuit with respect to footed DML and DMTGDI

counterparts at different process corners is shown in Fig. 4.7 (a) and Fig. 4.7 (b) respectively.




(a)

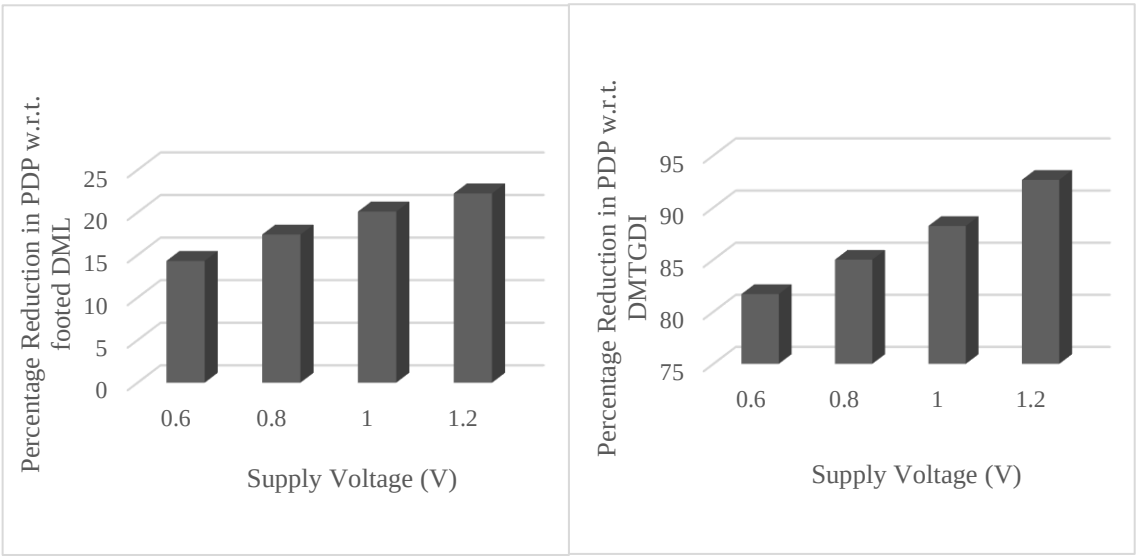



(b)

Fig. 4.7 Percentage reduction in total PDP in both static and dynamic mode for proposed 2-input gates and 1-bit FA circuit at five different process corners (a) with respect to footed DML design (b) with respect to DMTGDI design

As observed, for 2-input gates, a maximum PDP reduction of 33.52% and 96.61% is achieved using the proposed M-DMTGDI design as compared to their footed DML and DMTGDI counterparts. Corresponding values are 94.18% and 99.79% for a 1-bit FA circuit. It can be inferred that the proposed M-DMTGDI design is more adept at reducing total PDP of the design as compared to existing footed DML and DMTGDI designs.

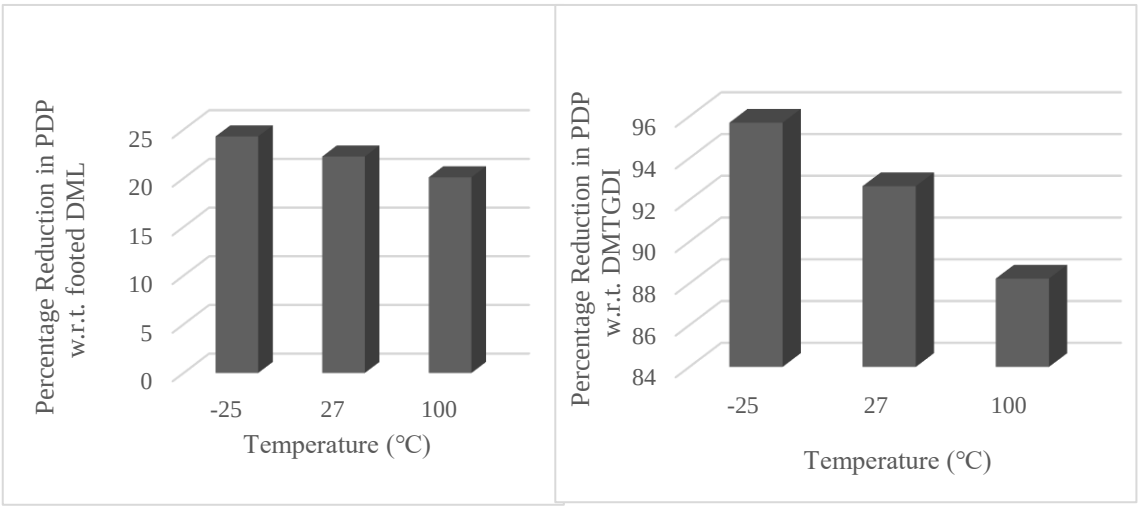
The efficacy of the proposed M-DMTGDI design is also investigated for 2-input NAND gate at different supply voltages (0.6 V-1.2 V) at 90nm. Figure 4.8 illustrates the percentage reduction in total PDP in both static and dynamic mode achieved using M-DMTGDI design as compared to their footed DML and DMTGDI counterparts. The efficacy of the proposed design at reducing PDP increases with increase in supply voltage.




(a) (b)

Fig. 4.8 Percentage reduction in total PDP in both static and dynamic mode for proposed M-DMTGDI design based 2-input type A NAND gate at different voltages (a) with respect to footed DML design (b) with respect to DMTGDI design

Further, the efficiency of the proposed M-DMTGDI design in terms of percentage PDP reduction is investigated for 2-input NAND gate at different temperatures i.e., -25 °C, 27 °C and 100 °C at 90nm in static and dynamic mode. Figure 4.9 illustrates the percentage reduction in total PDP in both static and dynamic mode achieved using M-DMTGDI design as compared to their footed DML and DMTGDI counterparts at different temperatures. It can be inferred that the proposed M-DMTGDI design offers total PDP reduction as compared to footed DML and DMTGDI designs across different temperature.




(a) (b)

Fig. 4.9 Percentage reduction in total PDP in both static and dynamic mode for proposed M-DMTGDI design based 2-input type A NAND gate at different temperature (a) with respect to footed DML design (b) with respect to DMTGDI design

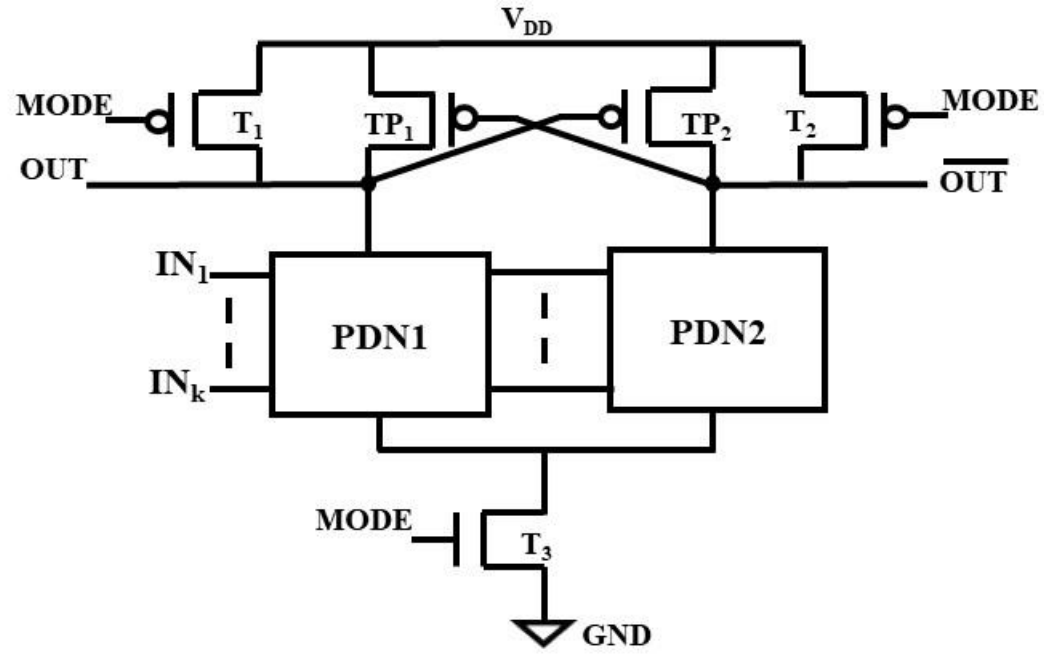
## 4.3 Proposed Design-IV: Dual Mode DCVSL

The DML design, akin to static CMOS, consists of PUN and PDN, complemented by additional transistors. The proposed design-IV, named DM-DCVSL, integrates dual-mode capability into the DCVSL design by incorporating two or more transistors in the existing static DCVSL design. To achieve both true and complemented outputs using the DML design, the number of transistors in PUN is doubled. However, the static DCVSL

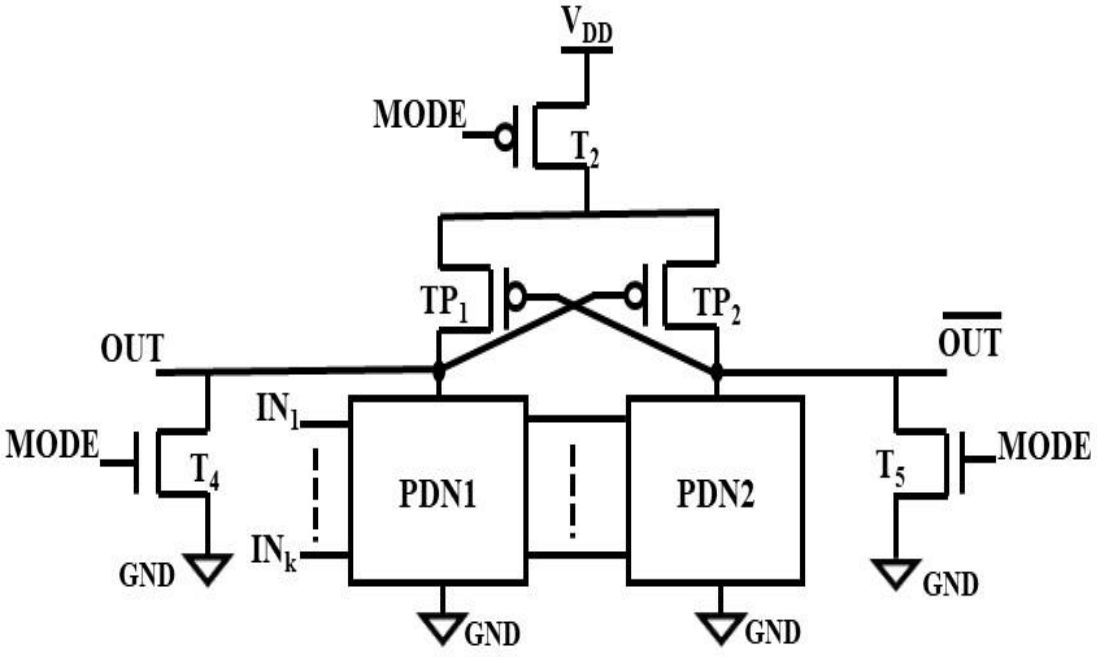
design produces differential outputs using fewer transistors, employing only one transistor in PUN. Therefore, the addition of dual-mode capability to the existing static DCVSL design using proposed design-IV enables obtaining differential outputs while utilizing fewer transistors.

### 4.3.1 Operation

To have dual mode logic operation i.e., static and dynamic mode in a single DCVSL design, a DM-DCVSL design is proposed by incorporating additional transistors in the existing static DCVSL design. The proposed design can exist in two types of topologies- type A and type B. The generalised structure of the proposed design for type A and type B topology is depicted in Fig. 4.10. Both topologies use two PDNs namely PDN1 and PDN2 which are mutually exclusive. Thus, if PDN1 conducts, PDN2 remains off and vice versa. The outputs OUT and $\overline{OUT}$ are complementary to each other. For type A topology, pre-charge ($T_1$, $T_2$) and footer transistor ($T_3$) are added while for type B design, pre-discharge ($T_4$, $T_5$) and header transistor ($T_2$) are added to the existing static DCVSL design. In proposed DM-DCVSL design, MODE input is constant logic “1” for type A topology and constant logic “0” signal for type B topology in static mode. For dynamic mode of operation, a clock signal, which allows pre-charge/pre-discharge and evaluation phases, is applied as MODE input.




(a)

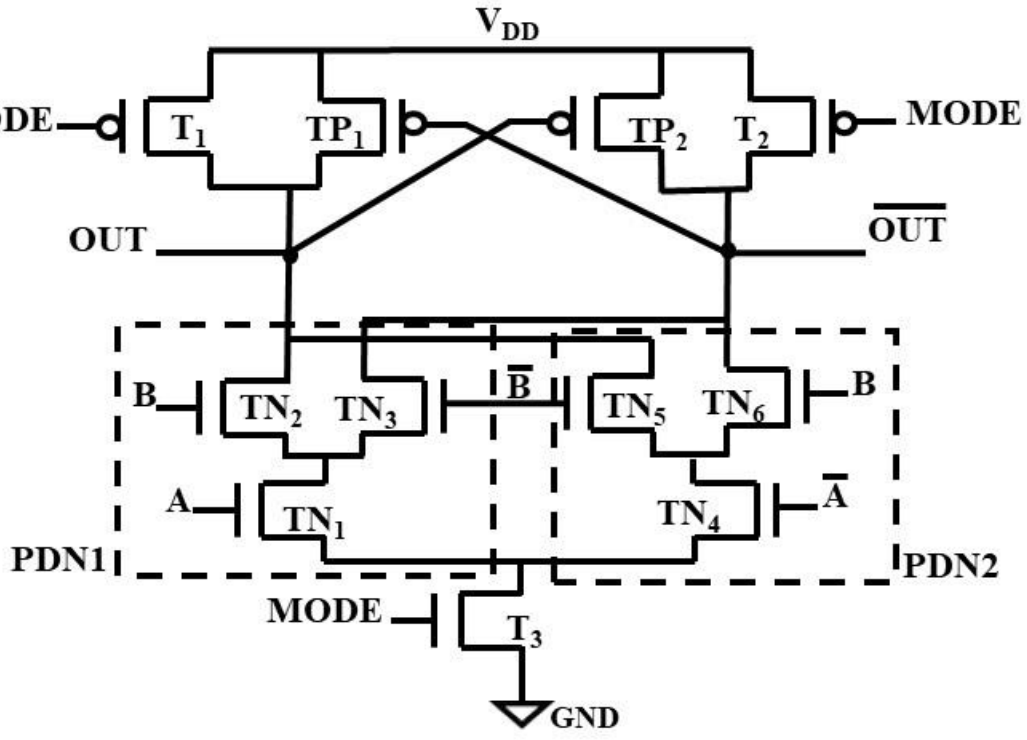



(b)

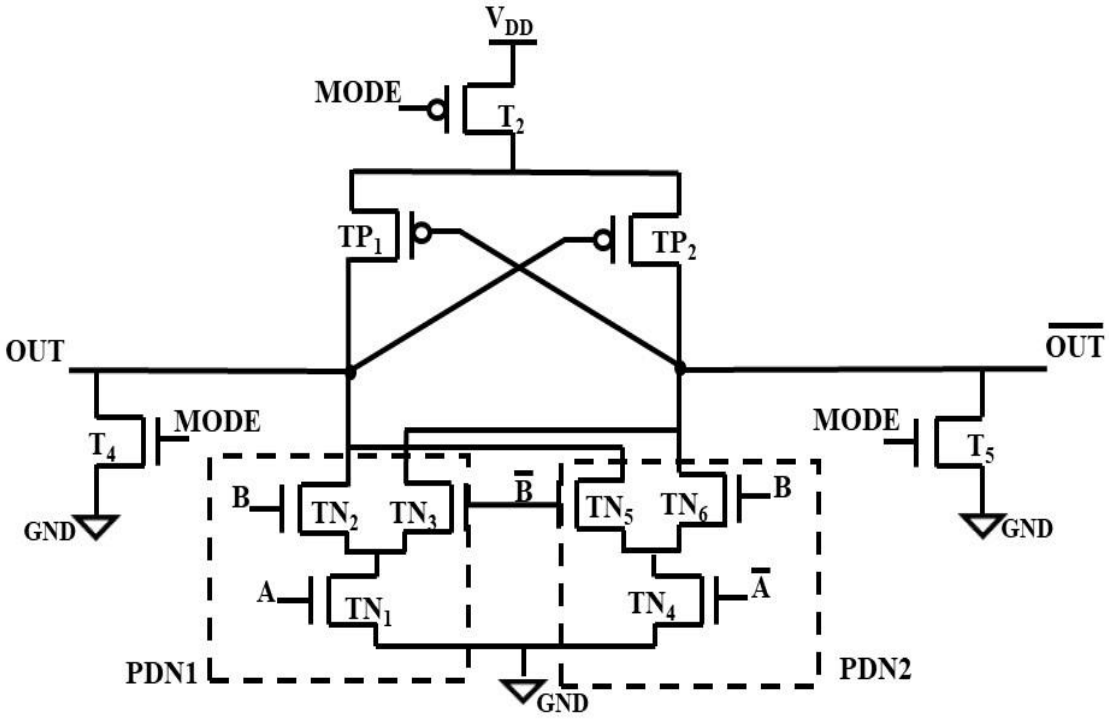
Fig. 4.10 Proposed DM-DCVSL design (a) Type A (b) Type B

To elucidate the proposed design, a 2-input type A DM-DCVSL XOR/XNOR gate is shown in Fig. 4.11 (a). Considering OUT and $\overline{OUT}$ are logic "1" and logic "0" respectively and PDN1 conducts for given set of inputs while PDN2 remains off. In this

case, PDN1 tries to pull down OUT though there is connection from $V_{DD}$ to OUT through $TP_1$ . The $\overline{OUT}$ is in high impedance state till the OUT drops to $V_{DD}$-$|V_{tP}|$. At this time, $TP_2$ charges $\overline{OUT}$ to logic "1" causing $TP_1$ to become off and finally OUT attains logic "0". Complementary inputs-A, $\overline{A}$ , B and $\overline{B}$ are applied to get complementary outputs-OUT and $\overline{OUT}$ . Using MODE input, the proposed design can be operated in both static and dynamic mode. In static mode (MODE=logic "1"), transistors $T_1$ and $T_2$ are off. The footer transistor $T_3$ is on, the circuit performs XOR (OUT) and XNOR ($\overline{OUT}$) logic operation according to the inputs applied. In dynamic mode, when the MODE is logic "0", the transistors $T_1$ and $T_2$ becomes on and charge the corresponding output nodes, OUT and $\overline{OUT}$ to $V_{DD}$. The footer transistor $T_3$ is off which prohibits discharging of output nodes. Subsequently when MODE is logic "1", the design enters in evaluation phase. Transistors $T_1$ and $T_2$ are turned off and the footer transistor $T_3$ is on, the complementary outputs are obtained according to the applied inputs.




(a)




(b)

Fig. 4.11 Proposed DM-DCVSL based 2-input XOR/XNOR gate (a) Type A (b) Type B

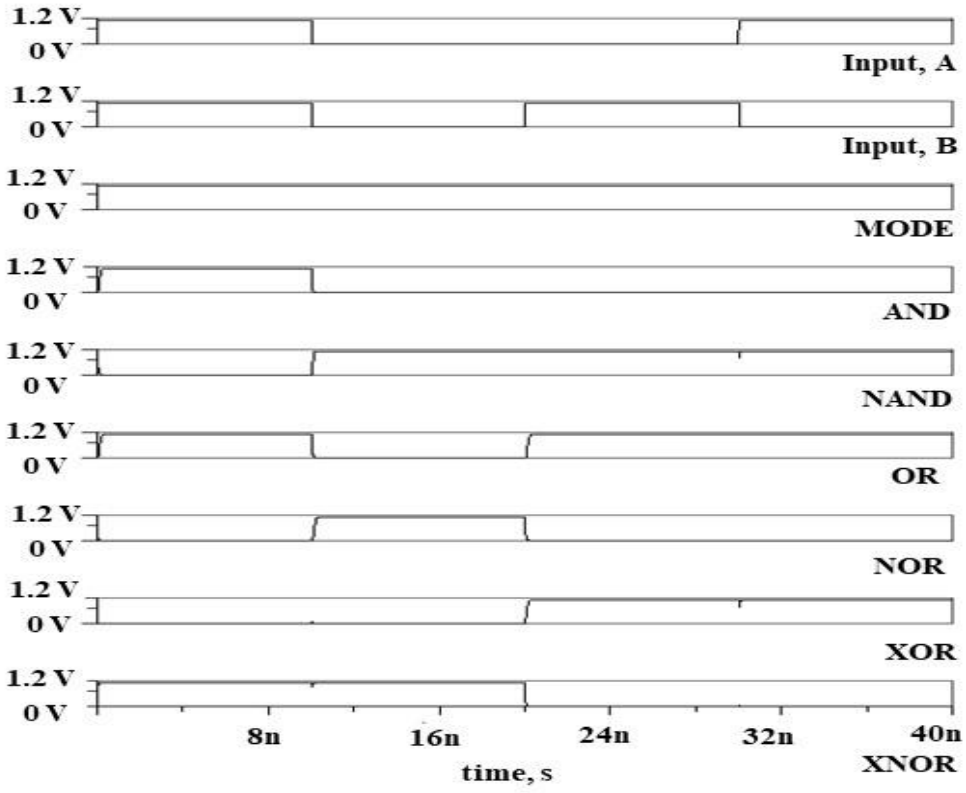
The proposed 2-input type B DM-DCVSL XOR/XNOR gate is shown in Fig. 4.11 (b) and the analysis is same as that of 2-input type A DM-DCVSL XOR/XNOR gate. The only difference is that here, in static mode, the MODE input is constant logic "0". Therefore, transistors $T_4$ and $T_5$ are turned off. The header transistor $T_2$ is on, the circuit performs XOR (OUT) and XNOR ($\overline{OUT}$) logic operation according to the inputs applied. In dynamic mode, for pre-discharge phase, MODE input is logic "1" which makes transistors $T_4$ and $T_5$ on. The header transistor $T_2$ is off which prohibits charging of output nodes. Both the outputs are pre-discharged to ground. For evaluation phase, the MODE input is logic "0", which makes transistors $T_4$ and $T_5$ off and header transistor $T_2$ on. The complementary outputs are obtained according to the applied inputs in the evaluation phase.

### 4.3.2 Simulation results

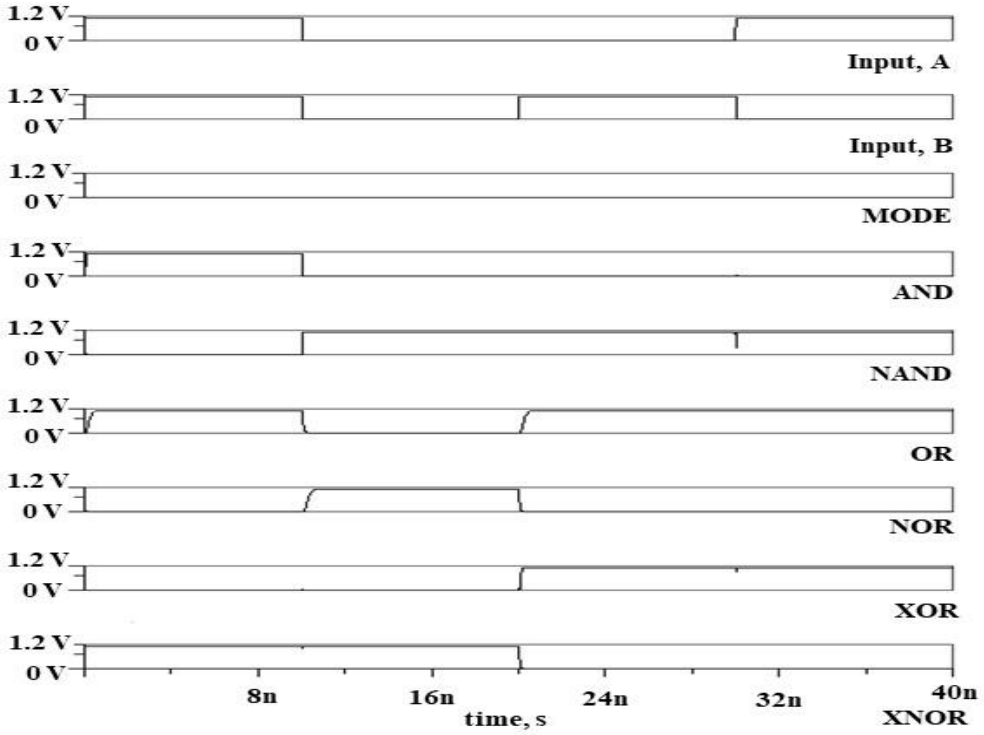
This section consists of two subsections namely functional verification to examine the working of the proposed DM-DCVSL design and performance analysis of the existing static DCVSL, dynamic DCVSL and proposed DM-DCVSL design in terms of power, delay, and PDP. The designs are simulated for 2-input AND/NAND, OR/NOR, XOR/XNOR gates and a 1-bit FA circuit. The simulations are performed using Symica DE tool at 1.2 V supply voltage and load capacitance of 5fF using 90nm BSIM4 model card for bulk CMOS. The SPICE simulator SymSpice is used to demonstrate the operation of proposed designs. SymProbe tool is used for power and delay analysis. Corner analysis is also done for all the circuits, both in static and dynamic mode. Effect of voltage and temperature variation is also investigated.

#### 4.3.2.1 Functional verification

The transient waveforms of 2-input gates- AND/NAND, OR/NOR, XOR/XNOR gates based on proposed DM-DCVSL design for type A and type B gates in static mode is depicted in Fig. 4.12. In the static mode of both type A and type B gates, a AND/NAND gate produces logic “1” at AND only when all inputs are logic “1”; otherwise, it is logic “0” .The output is logic “1” if any input is logic “0” for NAND while OR/NOR produces logic “1” output when any input is logic “1” for OR and NOR gives a logic “0” output if any input is logic “1”. An XOR/XNOR gate generates a logic “1” output if an odd number of inputs are logic “1”; otherwise, the output is logic “0” for XOR and the output is logic “1” if an even number of inputs are logic “1”; otherwise, it is logic “0” for XNOR. Thus, the simulated values align closely with the expected theoretical outcomes in the static mode.



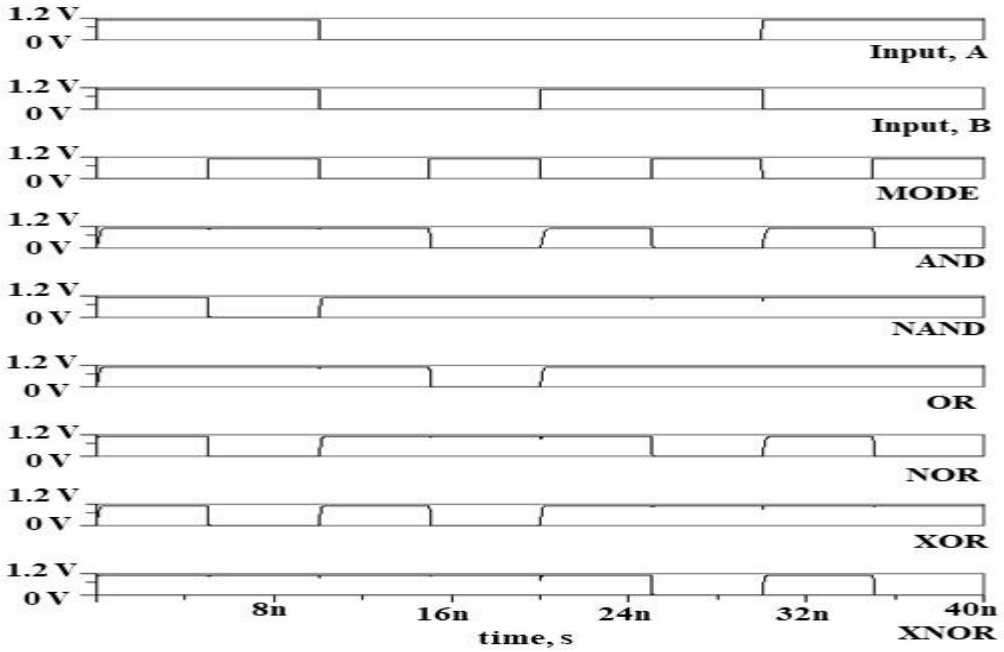

(a)



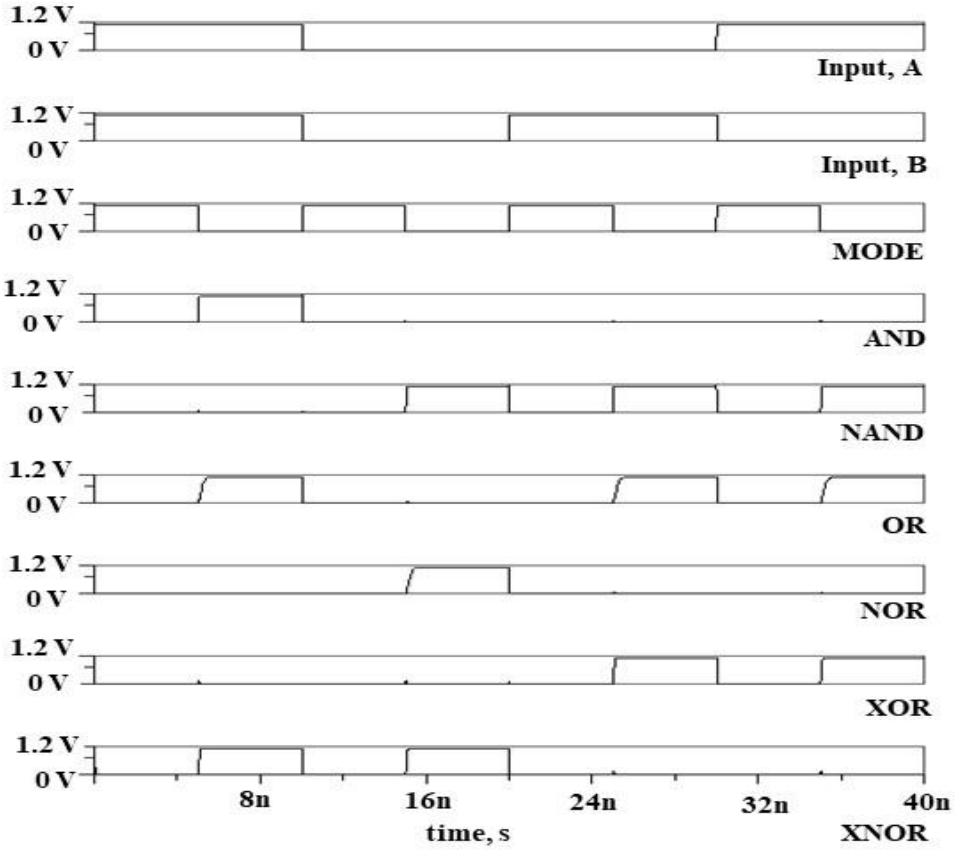

(b)

Fig. 4.12 Transient waveforms of proposed DM-DCVSL based 2-input gates at 90nm in static mode (a) Type A (b) Type B

Figure 4.13 illustrates the transient waveforms of 2-input gates - AND/NAND, OR/NOR, XOR/XNOR gates – implemented using the proposed DM-DCVSL design for both type A and type B topologies in dynamic mode. In the proposed DM-DCVSL design for type A gates, during the pre-charge phase, the MODE input is logic “0”, ensuring that the output of all gates is charged to the supply voltage. For type B gates, during pre-discharge phase, the MODE input is logic “1”, ensuring that the output of all gates is discharged to ground. Conversely, in the evaluation phase, the MODE input is logic “1” for type A gates and logic “0” for type B gates. Notably, during this phase, a AND/NAND gate produces logic “1” at AND only when all inputs are logic “1”; otherwise, it is logic “0” and the NAND output is logic “1” if any input is logic “0” while OR/NOR produces logic “1” output when any input is logic “1” for OR and logic “0” output if any input is logic “1” for NOR. An XOR/XNOR gate generates a logic “1” output for XOR if an odd number of inputs are logic “1”; otherwise, the output is logic “0” and XNOR is logic “1” if an even number of inputs are logic “1”. Consequently, the proposed DM-DCVSL-based AND/NAND, OR/NOR, XOR/XNOR gates operate correctly in dynamic mode.




(a)




(b)

Fig. 4.13 Transient waveforms of proposed DM-DCVSL based 2-input gates at 90nm in dynamic mode (a) Type A (b) Type B

Further, in order to show the cascading of type A and type B topologies of proposed DM-DCVSL design, a 1-bit FA circuit is also implemented. The sum block is implemented using type B topology and the carry block is implemented using type A topology. The applied input waveforms for inputs A,B,C and MODE input for type A (TA-MODE) and type B topology (TB-MODE) are depicted in Fig. 4.14 and Fig. 4.15 respectively. The transient waveforms for sum (SUM) and carry (CARRY) in static mode is depicted in Fig. 4.14. It may be noted that in static mode, the SUM bit is logic “1” when an odd number of logic “1” is present among the inputs and the CARRY bit is logic “1” when at least two of the three inputs are logic “1”.

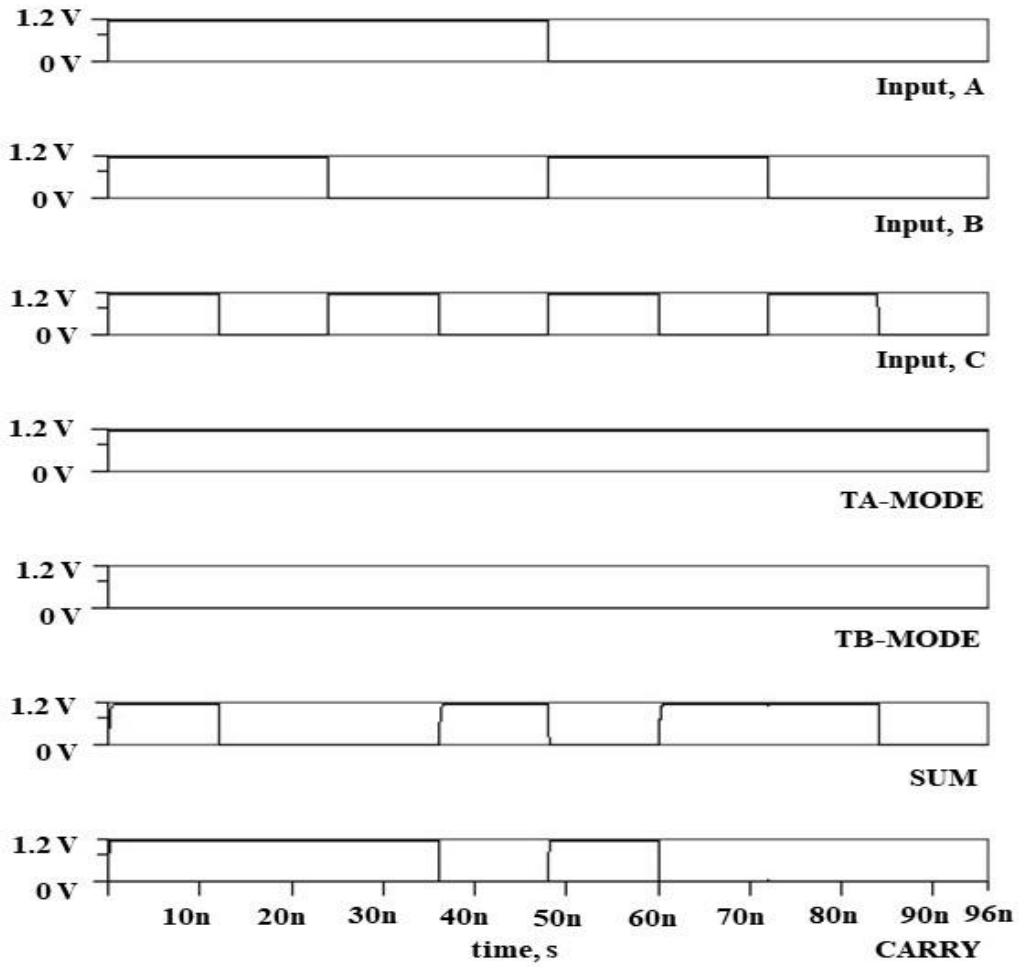



Fig. 4.14 Transient waveforms of proposed DM-DCVSL based 1-bit FA in static mode

The transient waveforms for sum (SUM) and carry (CARRY) in dynamic mode is depicted in Fig. 4.15. In pre-charge/pre-discharge phase of dynamic mode, since the sum block is type B, therefore MODE is logic “1” causing the SUM bit to be at logic “0”. Similarly, since the carry block is type A therefore MODE is logic “0” as a result the CARRY bit is logic “1”. During the evaluation phase, the SUM bit becomes logic “1” when there's an odd number of logic “1” inputs, while the CARRY bit is logic “1” if at least two out of the three inputs are logic “1”.

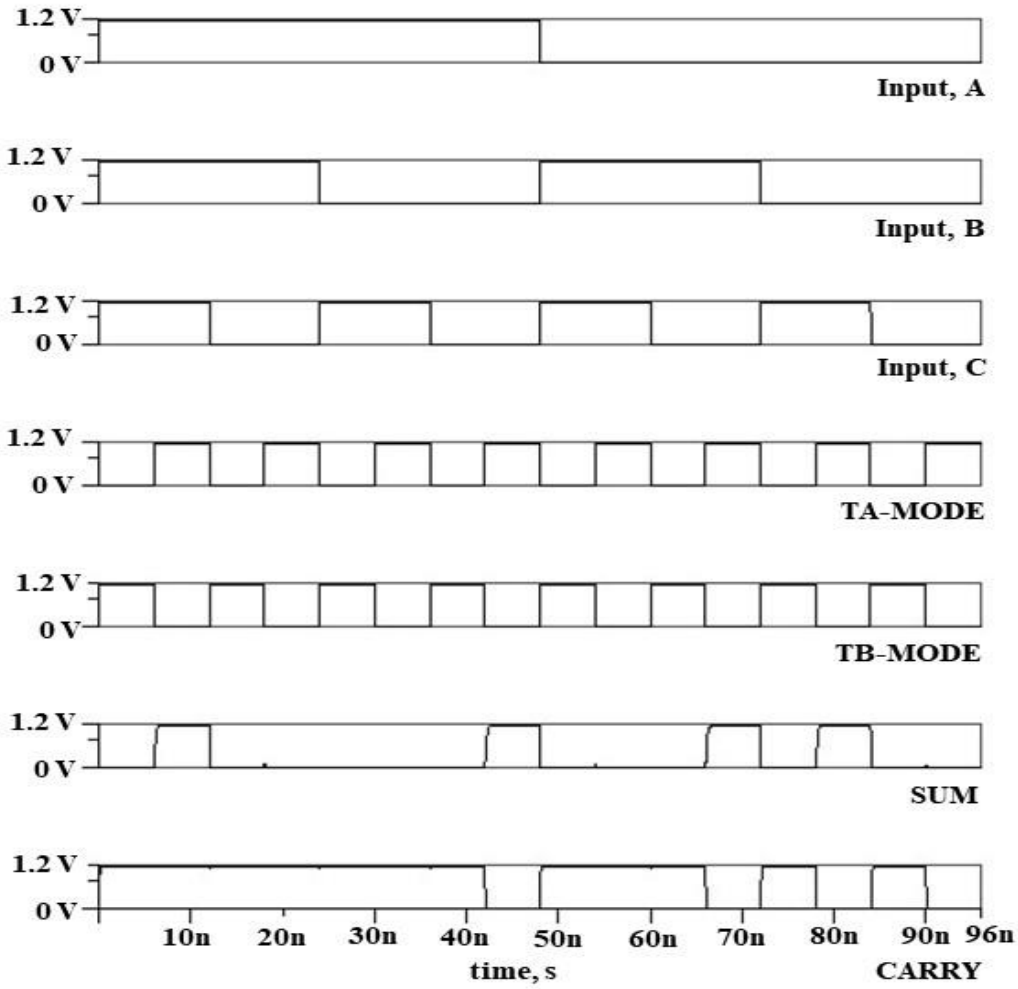



Fig. 4.15 Transient waveforms of proposed DM-DCVSL based 1-bit FA in dynamic mode

#### 4.3.2.2 Performance comparison

In this subsection, the performance comparison of the existing static and dynamic DCVSL and the proposed DM-DCVSL design is conducted using 2-input AND/NAND, OR/NOR, XOR/XNOR gates and a 1-bit FA circuit in terms of power, delay and PDP. The simulation is done using 90nm BSIM4 model card for bulk CMOS in Symica DE tool with 1.2 V supply voltage and a load capacitance of 5fF.

Tables 4.3 and 4.4 enlists the power, delay and PDP of the existing designs and the proposed DM-DCVSL based 2-input AND/NAND, OR/NOR, XOR/XNOR gates and a

1-bit FA circuit in static and dynamic mode respectively. Following are the observations based on Tables 4.3 and 4.4:

i. For type A gates, PDP reduction of 16.61%-58.63% is achieved and the corresponding values are 25.42%-95.51% for type B counterparts in static mode.

ii. For 1-bit FA, PDP reduction of 57.09% is achieved in static mode.

iii. The proposed DM-DCVSL design shows significant PDP reduction in static mode as compared to the existing static DCVSL counterparts.

iv. In dynamic mode, for type A gates, PDP reduction of 74.35%-84.71% is achieved and the corresponding values are 50.69%-97.44% for type B counterparts

v. For 1-bit FA, PDP reduction of 79.18% is achieved in dynamic mode.

vi. The reduction in PDP is notably higher when utilizing the proposed DM-DCVSL design in dynamic mode compared to static mode.

vii. Consequently, operating the proposed DM-DCVSL design in dynamic mode for over 50% longer duration than in static mode demonstrates significantly enhanced efficiency at PDP reduction compared to prolonged operation in static mode.

Table 4.3 Power, delay and PDP of proposed type A and type B DM-DCVSL in static mode and static DCVSL for 2-input gates and 1-bit FA at 90nm at 27°C

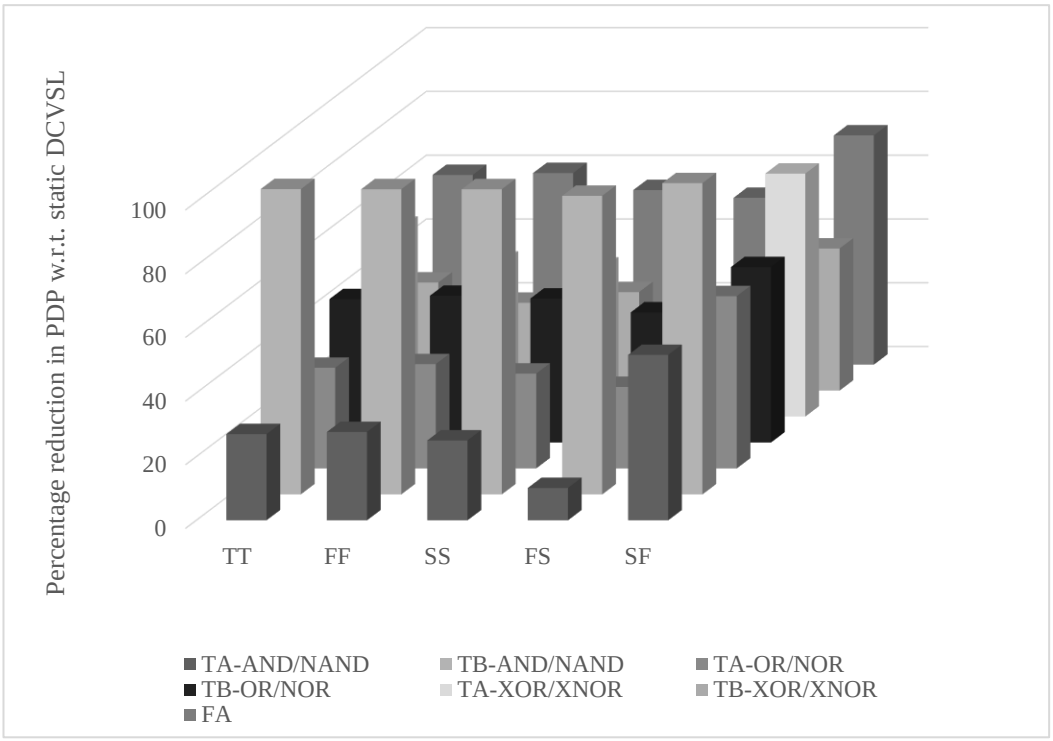
| Circuit | Parameter | Static DCVSL | Type A DM-DCVSL | Type B DM-DCVSL |
|---|---|---|---|---|
| AND/NAND | Power(uW) | 3.7 | 3.54 | 0.52 |
| | Delay(ps) | 74.84 | 62.1 | 23.93 |
| | PDP(aJ) | 276.91 | 219.83 | 12.44 |
| AND/NAND | Power(uW) | 3.7 | 3.54 | 0.52 |
| | Delay(ps) | 74.84 | 62.1 | 23.93 |
| | PDP(aJ) | 276.91 | 219.83 | 12.44 |
| OR/NOR | Power(uW) | 2.8 | 2.3 | 2.03 |
| | Delay(ps) | 86.14 | 73.8 | 68.84 |
| | PDP(aJ) | 241.19 | 169.74 | 139.75 |
| XOR/XNOR | Power(uW) | 2.08 | 1.46 | 2.03 |
| | Delay(ps) | 112.61 | 66.36 | 86.05 |
| | PDP(aJ) | 234.23 | 96.89 | 174.68 |
| FA | Power(uW) | 15.6 | 11.54 | 11.54 |
| | Delay(ps) | 160.26 | 92.97 | 92.97 |
| | PDP(aJ) | 2500.06 | 1072.87 | 1072.87 |

Table 4.4 Power, delay and PDP of proposed type A and type B DM-DCVSL in dynamic mode and dynamic DCVSL for 2-input gates and 1-bit FA at 90nm at 27℃

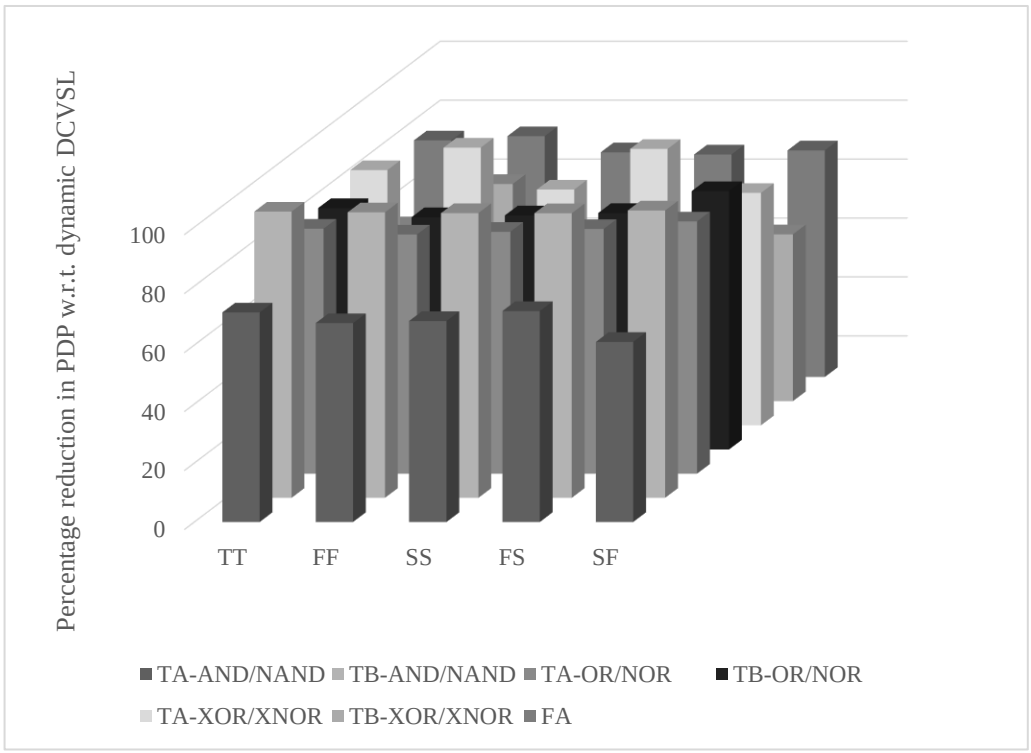
| Circuit | Parameter | Dynamic DCVSL | Type A DM-DCVSL | Type B DM-DCVSL |
|---|---|---|---|---|
| AND/NAND | Power(uW) | 7.91 | 8.43 | 0.78 |
| | Delay(ps) | 42.5 | 10.23 | 11.03 |
| | PDP(aJ) | 336.18 | 86.24 | 8.6 |
| OR/NOR | Power(uW) | 6.54 | 4.31 | 4.28 |
| | Delay(ps) | 40.91 | 11.74 | 11.94 |
| | PDP(aJ) | 267.55 | 50.6 | 51.1 |
| XOR/XNOR | Power(uW) | 7.39 | 4.74 | 7.4 |
| | Delay(ps) | 43.62 | 10.4 | 21.48 |
| | PDP(aJ) | 322.35 | 49.3 | 158.95 |
| FA | Power(uW) | 31.23 | 19.82 | 19.82 |
| | Delay(ps) | 95.66 | 31.38 | 31.38 |
| | PDP(aJ) | 2987.46 | 621.95 | 621.95 |

Further, the circuits are analysed at five different process corners i.e., TT, FF, SS, FS, SF to check the robustness of the proposed design at different process corners. Figures 4.16 (a) and 4.16 (b) illustrates the percentage reduction in PDP for proposed 2-input AND/NAND, OR/NOR, XOR/XNOR gates and a 1-bit FA circuit at five different process corners with respect to existing static DCVSL design in static mode and with respect to existing dynamic DCVSL design in dynamic mode.

Considering all process corners, it is observed that in static mode, a maximum PDP reduction of 97.7%, 55.09% and 76.23% for AND/NAND gate, OR/NOR gate and XOR/XNOR gate is achieved respectively. For a 1-bit FA circuit, the corresponding value is 71.9%. Similarly, in dynamic mode, a maximum PDP reduction of 97.48%, 87.64% and 94.21% for AND/NAND gate, OR/NOR gate and XOR/XNOR gate is achieved, respectively. For a 1-bit FA circuit, the corresponding value is 81.7%. Therefore, it can be inferred that the proposed design is effective in minimising the PDP of the existing DCVSL design at all process corners in both static and dynamic mode.



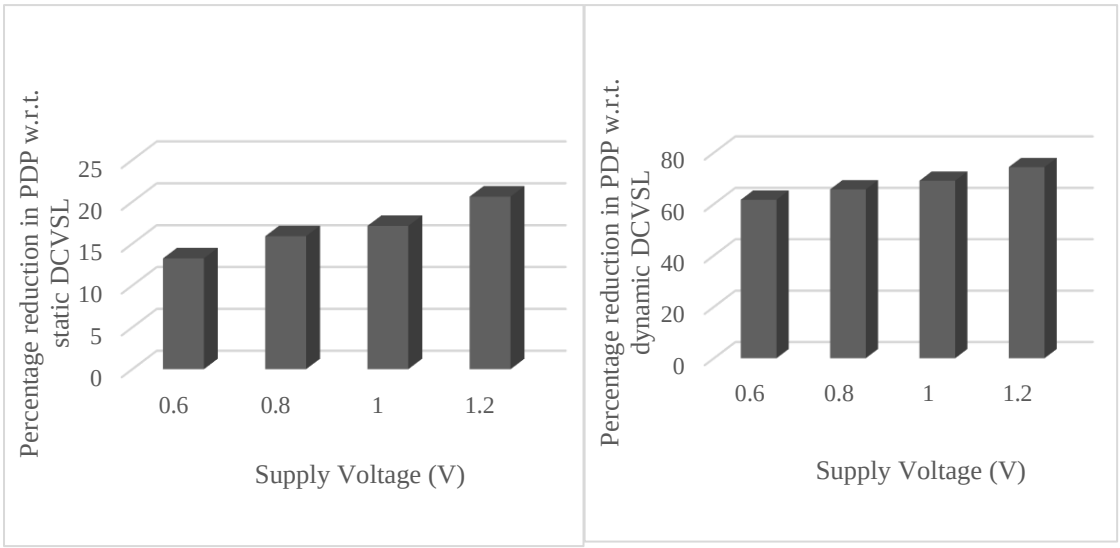

(a)




(b)

Fig. 4.16 Percentage reduction in PDP for proposed 2-input gates at five different process corners (a) Static mode w.r.t. static DCVSL (b) Dynamic mode w.r.t. dynamic DCVSL

The efficacy of the proposed DM-DCVSL design is also investigated for 2-input type A AND/NAND gate at different supply voltages (0.6 V-1.2 V) at 90nm. Figure 4.17 illustrates the percentage reduction in PDP in static mode with respect to static DCVSL and the percentage reduction in PDP in dynamic as compared to dynamic DCVSL at different supply voltage. It can be observed that the proposed design can reduce PDP at different supply voltage as well in both static and dynamic mode.

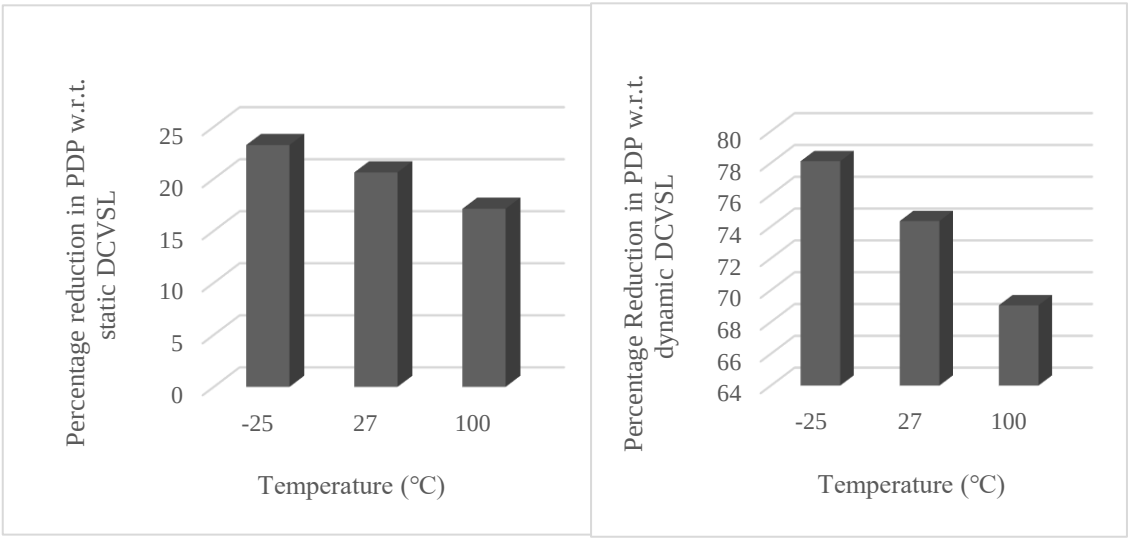



(a) (b)

Fig. 4.17 Percentage reduction in PDP for proposed DM-DCVSL based 2-input type A AND/NAND gate at different voltages (a) Static mode (b) Dynamic mode

Further, the efficiency of the proposed M-DMTGDI design in terms of percentage reduction in PDP is investigated for 2-input type A AND/NAND gate at different temperatures i.e., -25 °C, 27 °C and 100 °C at 90nm in static and dynamic mode. Figure 4.18 illustrates the percentage reduction in PDP in static mode with respect to static DCVSL and the percentage reduction in PDP in dynamic as compared to dynamic DCVSL at different temperature. It can be observed that the proposed DM-DCVSL

offers PDP reduction across different temperature as well as compared to its static DCVSL and dynamic DCVSL counterparts.




(a) (b)

Fig. 4.18 Percentage reduction in PDP for proposed DM-DCVSL based 2-input type A AND/NAND gate at different temperatures (a) Static mode (b) Dynamic mode

## 4.4 Conclusion

In this chapter, dual mode logic operation is achieved in existing designs by proposing two novel designs- M-DMTGDI and DM-DCVSL. Proposed design-III i.e. M-DMTGDI design provides dual mode operation while addressing the contention issue in the existing DMTGDI design. Proposed design-IV i.e. DM-DCVSL design introduces dual mode logic in existing static DCVSL design with fewer transistors. Extensive simulative investigation is done to analyse the proposed designs in terms of power, delay and PDP, while also checking the robustness of the proposed designs at different process corners and analysing the effect of variation of voltage and temperature. Using M-DMTGDI design, for 2-input gates, a maximum PDP reduction of 33.07% and 97.38% as compared to their footed DML and DMTGDI counterparts is achieved. For 1-bit FA

circuit, the corresponding values are 87.19% and 99.79%. For DM-DCVSL design, the maximum PDP reduction is 95.51% for 2-input gates in static mode and 97.44% in dynamic mode. For the 1-bit FA, the PDP reduction is 57.09% in static mode and 79.18% in dynamic mode. All simulation results are pre-layout, though post-layout results may vary by 10-15%. The proposed M-DMTGDI and DM-DCVSL are efficient at reducing PDP across different temperature, voltage and process corners. Comparative analysis shows that the proposed DM-DCVSL design provides PDP reduction in both static and dynamic mode, but the proposed M-DMTGDI design is adept at PDP reduction only when operated in dynamic mode for longer duration. Thus, M-DMTGDI exhibits higher performance for applications wherein the device is predominantly operated in dynamic mode of operation.

# Chapter 5

# Improved Transistor Technology Based Designs

The contents of this chapter are published in:

[1] N. Yadav, N. Pandey and D. Nand, **"Energy Efficient CNTFET based Dual Mode Logic (C-DML) Design,"** 2023 Second International Conference on Electrical, Electronics, Information and Communication Technologies (ICEEICT), Trichirappalli, India, 2023, pp. 1-6, doi: 10.1109/ICEEICT56924.2023.10157144.

[2] N. Yadav, N. Pandey and D. Nand, **"CNTFET Based MDMTGDI (C-MDMTGDI) Design and Its Leakage Analysis,"** 2023 10th International Conference on Signal Processing and Integrated Networks (SPIN), Noida, India, 2023, pp. 515-521, doi: 10.1109/SPIN57001.2023.10116812.

[3] N. Yadav, N. Pandey and D. Nand, **"CNTFET based Transmission Gate Diffusion Input Logic (C-TGDI) design,"** 2021 5th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT), Mysuru, India, 2021, pp. 701-705, doi: 10.1109/ICEECCOT52851.2021.9707944.

## 5.1 Introduction

The preceding chapters dealt with various alternative logic styles based on MOSFET technology. These MOSFET-based designs face several challenges, including increased leakage current, greater parametric variations, various short-channel effects, elevated heat generation, and reduced gate control [38-39]. Building on these challenges, this chapter presents two alternative logic styles: CNTFET based footed DML and M-DMTGDI design, which utilize CNTFETs, referred to as C-DML and C-MDMTGDI respectively. Further, leakage reduction techniques-LECTOR, GALEOR and LCNT are also explored for CNTFET based M-DMTGDI design.

## 5.2 Improved transistor technology- CNTFET overview

The CNTFET is a type of FET that replaces bulk silicon, which is used in conventional MOSFET designs, with one or more CNTs as the channel [36-40]. A graphite sheet is rolled up and wrapped around a vector, known as the chiral vector, which is governed by (m,n) chiral indices, to form a CNT [37].

The threshold voltage ($V_{thc}$) of CNTFET is determined by chiral indices (m,n) and the diameter of CNT [37], given by (5.1).

$$V_{thc} = \frac{0.43}{DCNT(nm)} \tag{5.1}$$

where DCNT is the diameter of CNT in nm.

The diameter of CNT, DCNT, in turn, depends on the chiral indices (m,n), given by (5.2) [37].

$$DCNT = \frac{\sqrt{3}a0\sqrt{m^2+mn+n^2}}{\pi} \tag{5.2}$$

where, a0 = 0.142 nm, $\pi = 3.14$

As a result, CNTFETs offer a special potential for threshold voltage adjustment by altering the CNT's diameter [44]. It has been demonstrated that CNTFETs have MOSFET-like characteristics [44]. Similar to MOSFETs, CNTFETs can be of N-type (N-CNTFET) and P-type (P-CNTFET). The ON current in CNTFET ($I_{on}$) [122] is approximately given by (5.3).

$$I_{on} \approx \frac{N g_{CNT}(VDD - V_{thc})}{1 + g_{CNT} L_s \rho_s} \tag{5.3}$$

where N: No. of CNTs per device,

$g_{CNT}$: Transconductance per CNT,

$V_{DD}$: Supply voltage,

$V_{thc}$: Threshold voltage of the CNTFET,

$L_s$: Source length,

$\rho_s$: Source resistance per unit length

A standard CNTFET based inverter, which consists of a P-CNTFET ($CP_1$) and N-CNTFET ($CN_1$) is shown in Fig. 5.1.

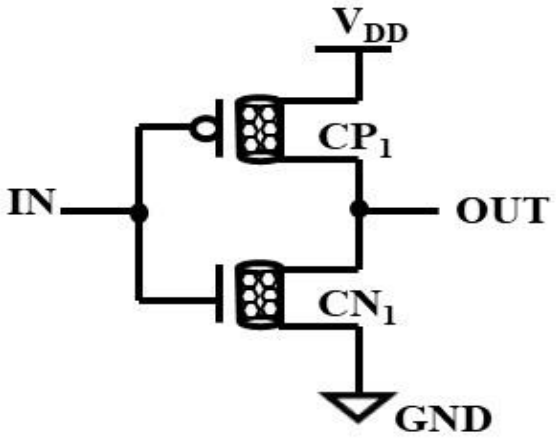
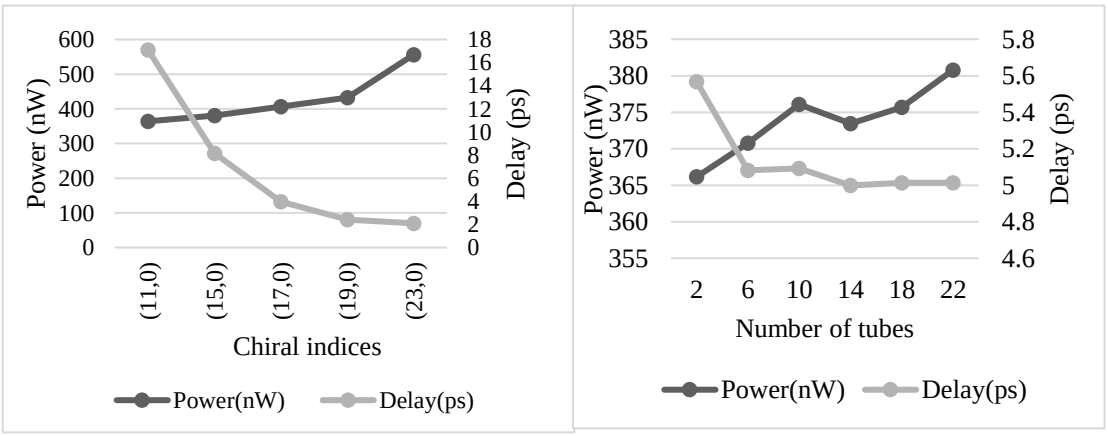



Fig. 5.1 Standard CNTFET based inverter [117]

The chiral indices and the number of tubes in the CNTFET device impacts the power and delay of the circuit [122]. The impact of variation of chiral indices and number of tubes for CNTFET based inverter is shown in Fig. 5.2. The ON current of CNTFET increases with increasing chiral indices which results in increased power and reduced delay. With increasing number of tubes, the power shows an upward trend while delay displays downward trend. It is direct consequence of enhanced ON current due to an increase number of tubes.



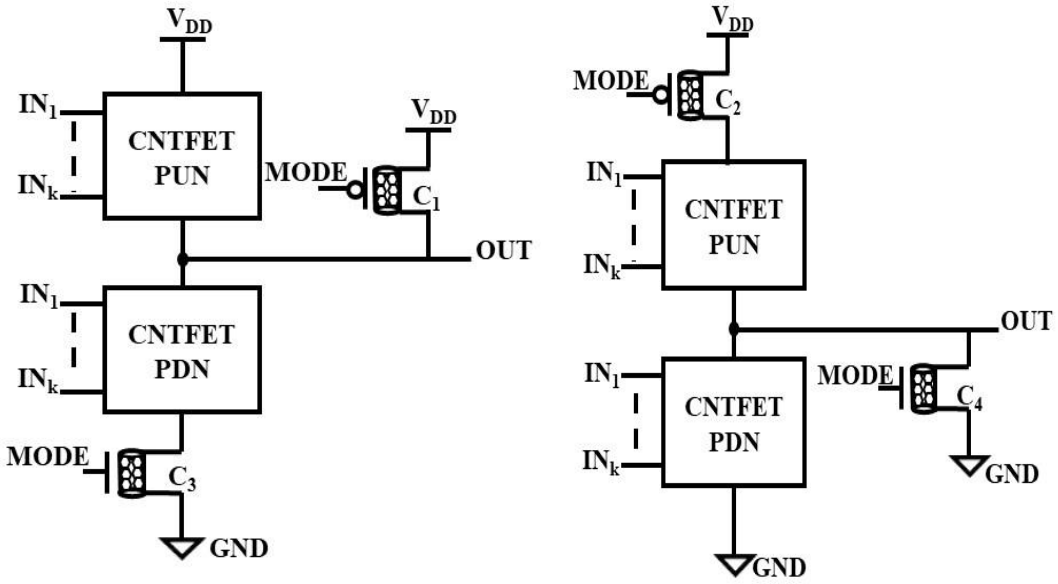

(a) (b)

Fig. 5.2 Power and delay for standard CNTFET based inverter at 32nm with variation in (a) Chiral indices (b) Number of tubes

## 5.3 Proposed Design-V: CNTFET based DML (C-DML)

The CMOS based footed DML logic style exists in open literature [14-15] and is deliberated in preceding chapters. The proposed design-V, referred to as C-DML, introduces a footed DML design that leverages CNTFETs to harness their advantages for its implementation. By introducing additional pre-charge/pre-discharge transistor and footer/header transistor, the existing static CNTFET design [39], consisting of PUN and PDN, is transformed into C-DML design. By changing the MODE input, the proposed design-V enables a circuit to operate in either static or dynamic mode. Figure 5.3 (a) and 5.3 (b) depicts the basic architecture of the two topologies of a C-DML design. A

pre-charge transistor ($C_1$) and a footer transistor ($C_3$) are added to the existing static CNTFET design to create a type A C-DML gate as shown in Fig. 5.3 (a). A header transistor ($C_2$) and a pre-discharge transistor ($C_4$) are added to the existing static CNTFET design to create a type B C-DML gate, as shown in Fig. 5.3 (b). For static mode, type A and type B gates are applied with a constant logic "1" and logic "0", respectively, as the MODE input. For dynamic mode, a clock signal is applied as the MODE input allowing operations in pre-charge/pre-discharge and evaluation phases. In type A design, the output node is charged to supply voltage during the pre-charge phase as MODE input is logic "0". For type B design, the output node is discharged to ground during the pre-discharge phase as MODE input is logic "1". During the evaluation phase, the output is evaluated according to the logic function in both type A and type B design.




(a) (b)

Fig. 5.3 Proposed C-DML design (a) Type A (b) Type B

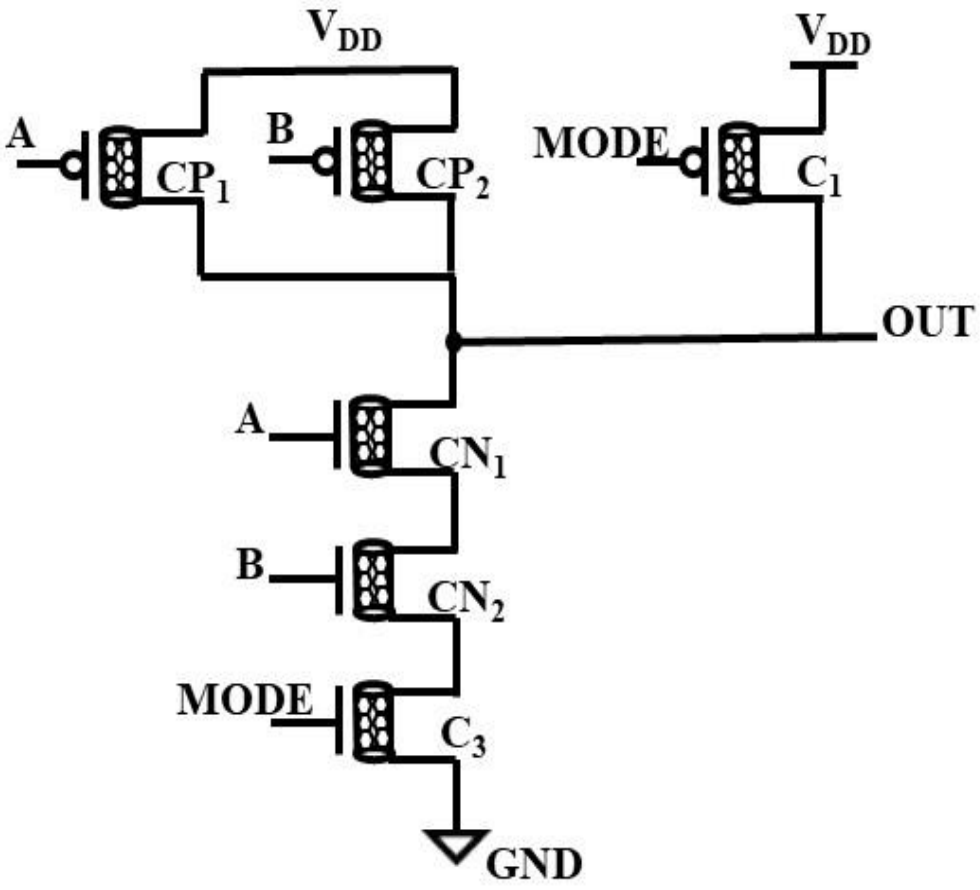
### 5.3.1 Operation

The proposed C-DML based 2-input type A NAND gate is shown in Fig. 5.4 (a). In static mode, the pre-charge transistor $C_1$ is off, and the footer transistor $C_3$ is on. When (A,B) = (1,1), both transistors $CN_1$, $CN_2$ are on, and transistors $CP_1$, $CP_2$ are off. This creates a path from output to ground and the output is logic "0". When the input (A,B) = (0,0), both transistors $CN_1$, $CN_2$ are off and simultaneously, transistors $CP_1$, $CP_2$ are on. This establishes a path between output node and $V_{DD}$, resulting in a logic "1" output . Similarly, in the case of (A, B)=(0, 1), $CP_1$ and $CN_2$ transistors are on, while $CN_1$ and $CP_2$ transistors are off. Consequently, the output becomes charged to $V_{DD}$ through transistor $CP_1$. When (A, B)= (1, 0), the $CP_1$ and $CN_2$ transistors are off, while $CN_1$ and $CP_2$ transistors are on. Consequently, a path is created between output node and $V_{DD}$, which makes output as logic "1".

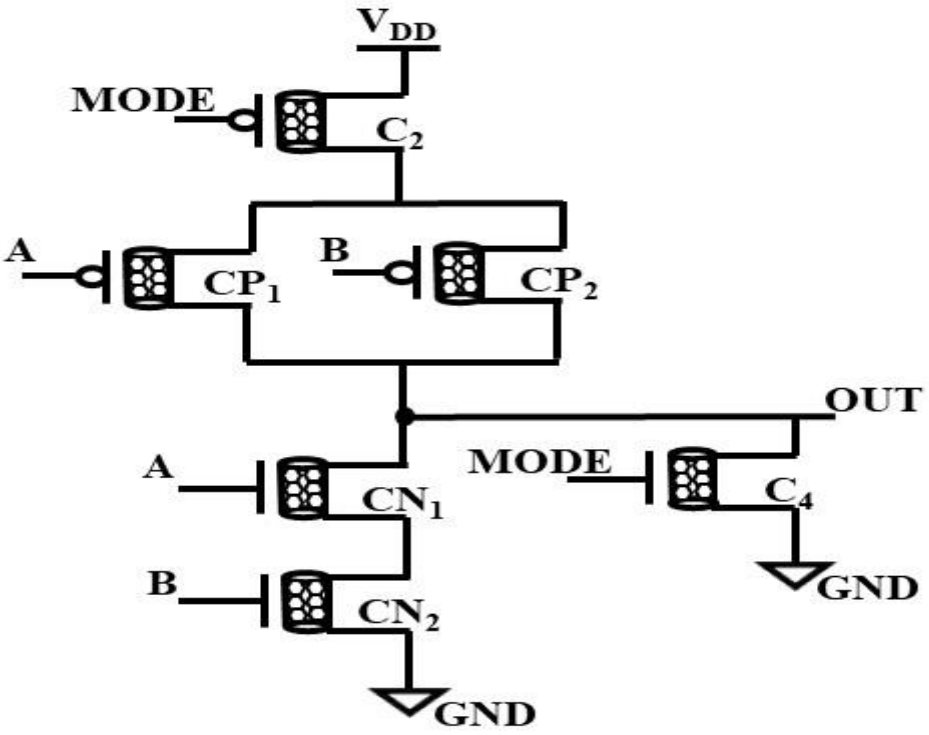
The operation of proposed C-DML based 2-input type A NAND gate in dynamic mode is elucidated next. In pre-charge phase, transistor $C_1$ becomes on as MODE input is logic "0" and the footer transistor $C_3$ is off. So, the output is fully charged to $V_{DD}$ as there is no path between output and ground. In evaluation phase (MODE= logic "1"), the pre-charge transistor $C_1$ is off, footer transistor $C_3$ is on, and the output is evaluated according to the inputs applied. For inputs (A, B) = (1, 1), transistors $CN_1$, $CN_2$ are on, and transistors $CP_1$, $CP_2$ are off causing a path to be created from output to ground. As a result, output becomes logic "0". When (A, B) = (0, 0), transistors $CN_1$, $CN_2$ are off, and transistors $CP_1$, $CP_2$ are on, the output is logic "1" due to a connection between output and $V_{DD}$ in this case. Similarly, with (A, B) = (0, 1), $CP_1$ and $CN_2$ transistors are on, while $CN_1$ and $CP_2$ transistors are off, establishing a path between the output and $V_{DD}$ to make output as logic "1". Lastly, for (A, B) = (1, 0), $CP_1$ and $CN_2$ transistors are off, while $CN_1$ and $CP_2$ transistors are on, creating an output to $V_{DD}$ connection which makes output as

logic “1”. It is thus clear that the C-DML type A design of Fig. 5.4 (a) adheres to NAND functionality in both static mode and dynamic mode.

Similar analysis can be done for proposed C-DML based 2-input type B NAND gate in static and dynamic mode, as depicted in Fig. 5.4 (b). In static mode, the pre-discharge transistor $C_4$ is off, header transistor $C_2$ is on and the output is evaluated according to applied inputs. In pre-discharge phase of dynamic mode, the header transistor $C_2$ is off and the pre-discharge transistor $C_4$ is on and it discharges the output node to ground. In evaluation phase, the NAND gate output is evaluated according to applied inputs, as the pre-discharge $C_4$ is off and header transistor $C_2$ is on.



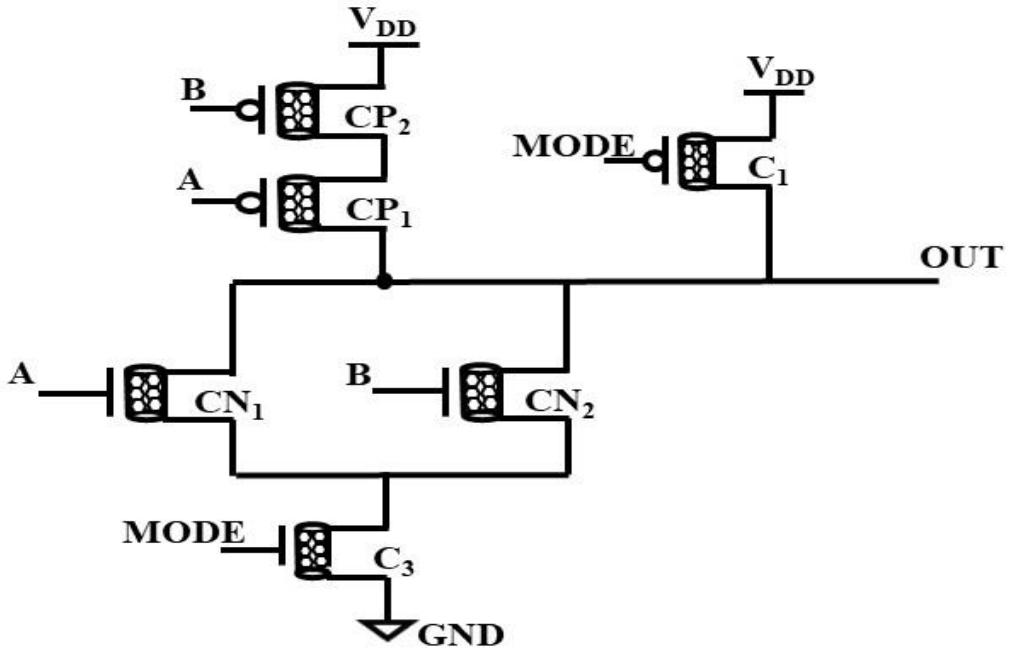

(a)



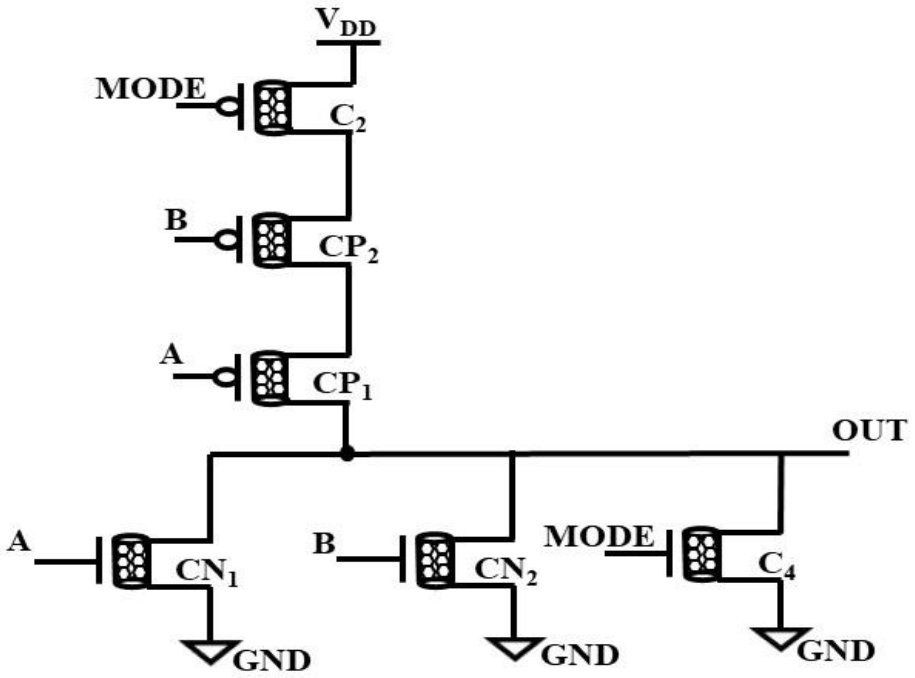

(b)

Fig. 5.4 Proposed C-DML based 2-input NAND gate (a) Type A (b) Type B

For the sake of completion, 2-input NOR and 2-input XOR gate designed using proposed type A and type B C-DML design, are depicted in Fig. 5.5 and Fig. 5.6 respectively.

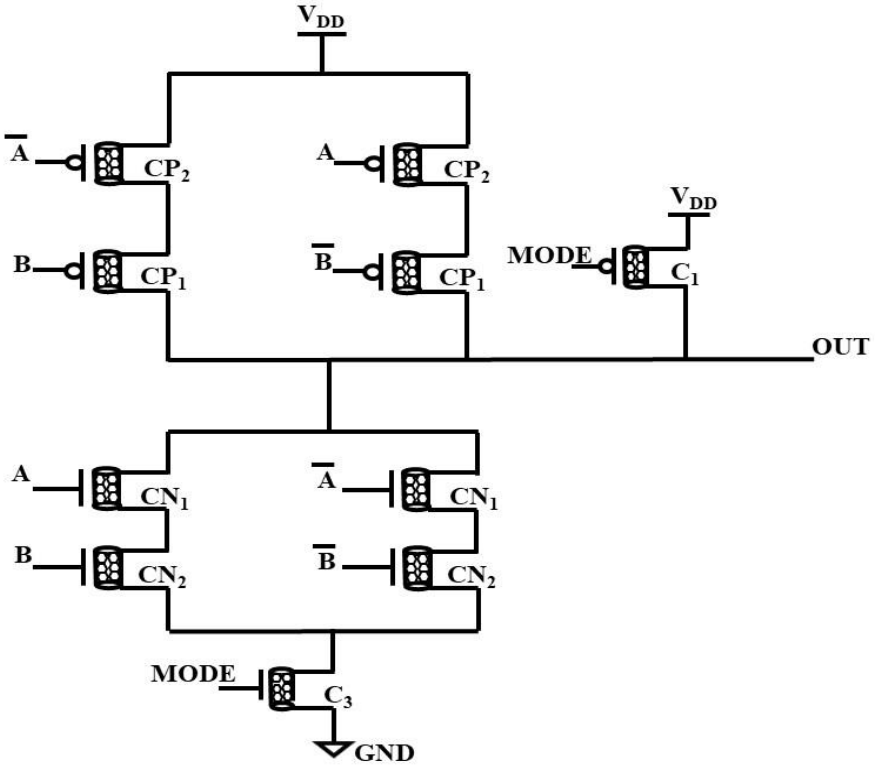



(a)

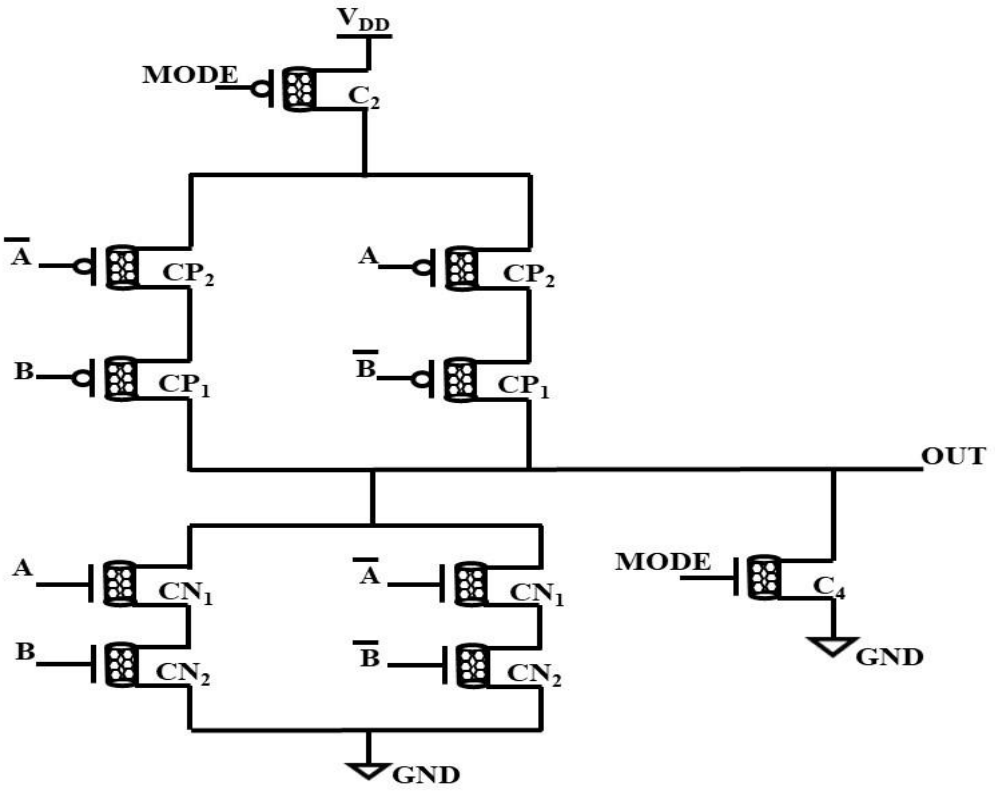



(b)

Fig. 5.5 Proposed C-DML based 2-input NOR gate (a) Type A (b) Type B




(a)




(b)

Fig. 5.6 Proposed C-DML based 2-input XOR gate (a) Type A (b) Type B

Further, a 1-bit FA circuit is also designed using type A and type B topology of proposed C-DML design using the schematic shown in Fig. 3.5. The 2-input NOR, 2-input XOR and 1-bit FA circuits are also analysed in similar manner. However, the discussion is omitted here for the sake of brevity.

### 5.3.2 Simulation results

This section is divided into two parts- the first part deals with the functional verification while the second part compares the performance of 2-input NAND gate, 2-input NOR gate, 2-input XOR gate and 1-bit FA based on proposed C-DML design with their CMOS based footed DML counterparts. The simulations are carried out using HSPICE tool with 32nm CNTFET Stanford model and 32nm BSIM4 model card for bulk CMOS at 0.9V supply voltage and a load capacitance of 5fF. The proposed C-DML

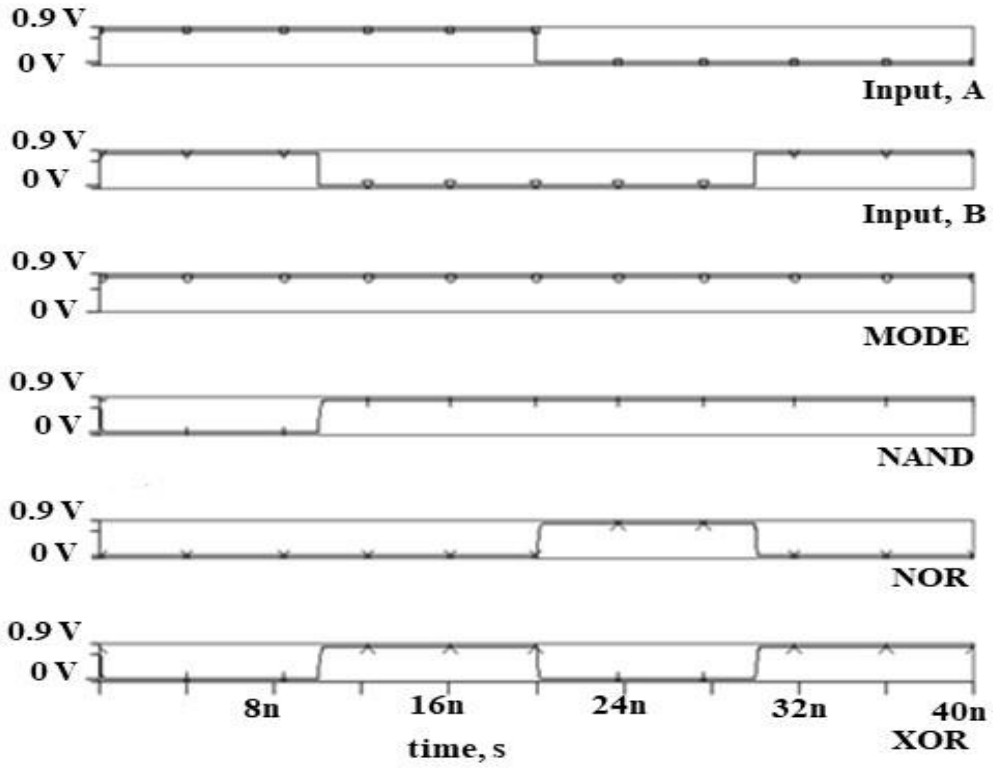
designs are constructed with a chiral indices of (13,0).

#### 5.3.2.1 Functional verification

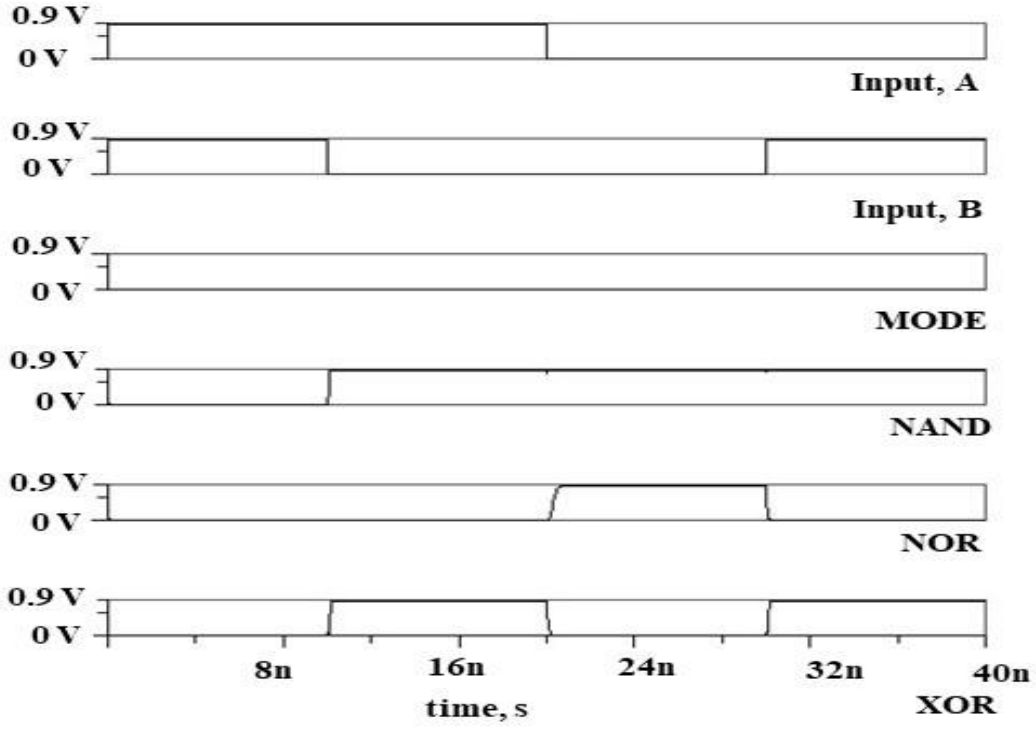
The transient waveforms of 2-input gates- NAND, NOR and XOR gates designed using proposed type A and type B C-DML design in static mode are shown in Fig. 5.7. Here, the MODE input is logic “0” for type A gates and logic “1” for type B gates. It may be noted that in static mode of both type A and type B gates, NAND gate gives an output of logic “1” if any of its inputs is logic “0”, while a NOR gate yields an output of logic “0” if any of its inputs is logic “1”. On the other hand, a XOR gate produces an output of logic “1” when its inputs differ and an output of logic “0” when inputs are same. Thus, the  values match well with the theoretical results in static mode.

The transient waveforms of 2-input gates, NAND, NOR and XOR, implemented using proposed type A and type B C-DML design in dynamic mode are shown in Fig. 5.8. In dynamic mode, the MODE input is connected to a clock signal having two phases of operation- pre-charge and evaluation. For proposed C-DML based type A gates, MODE input is logic “0” in pre-charge phase, so the output is charged to supply voltage for all gates. Alternatively, in evaluation phase, the MODE input is logic “1”. It may be noted that in evaluation phase, NAND gate gives an output of logic “1” if any of its inputs is logic “0”, while a NOR gate yields an output of logic “0” if any of its inputs is logic “1”. On the other hand, a XOR gate produces an output of logic “1” when its inputs differ and an output of logic “0” when inputs are same. Thus, proposed C-DML based NAND, NOR and XOR gates function correctly in dynamic mode.

Similar analysis can be done for proposed C-DML based type B gates in dynamic mode, with the only difference being that during the pre-discharge phase, the output node is discharged as MODE input is logic “1”, and during the evaluation phase, the MODE input is logic “0”.

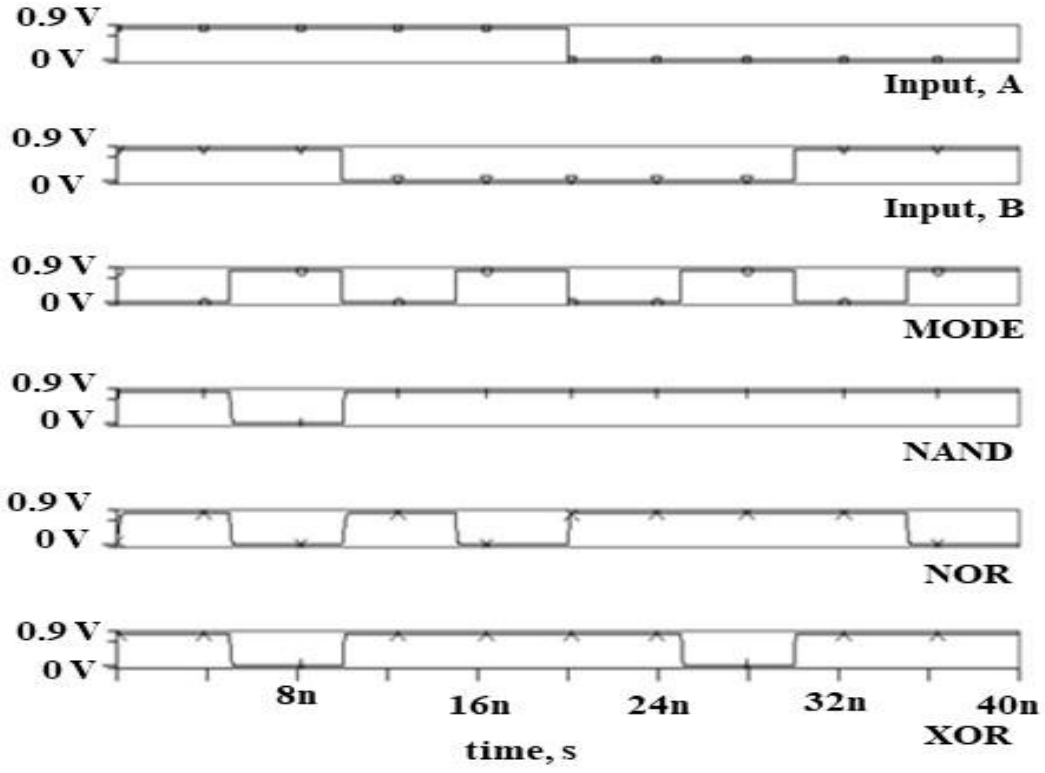



(a)

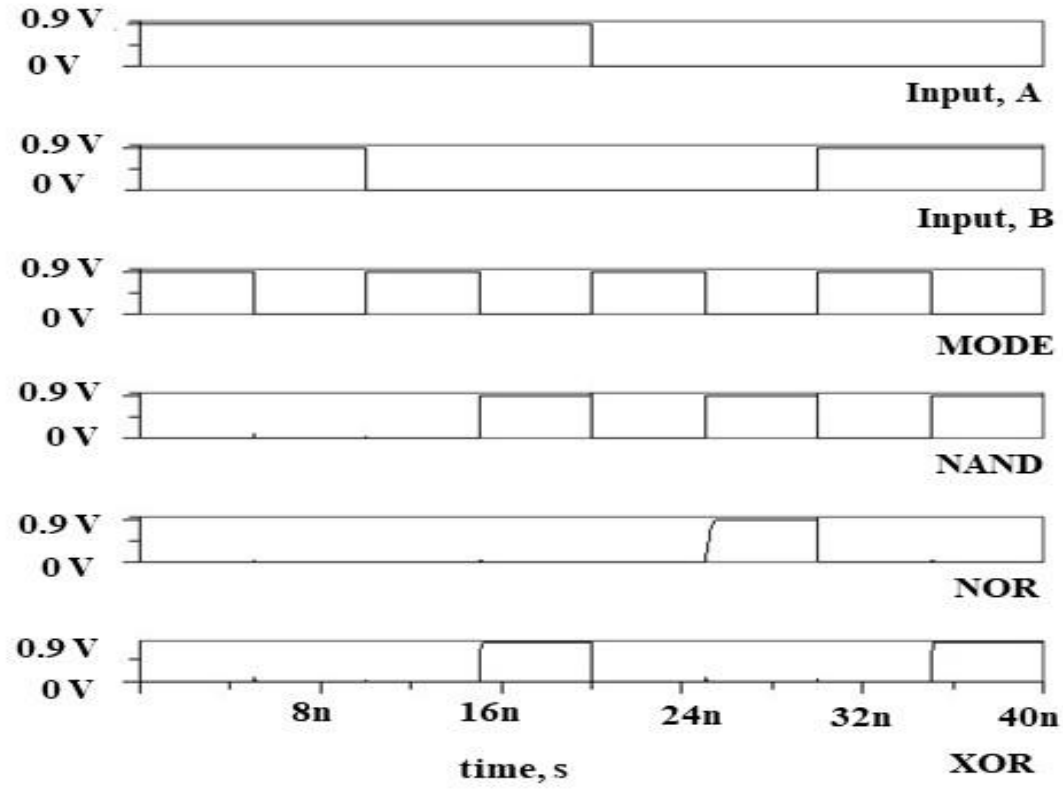



(b)

Fig. 5.7 Transient waveforms of proposed C-DML based 2-input gates at 32nm in static mode (a) Type A (b) Type B




(a)

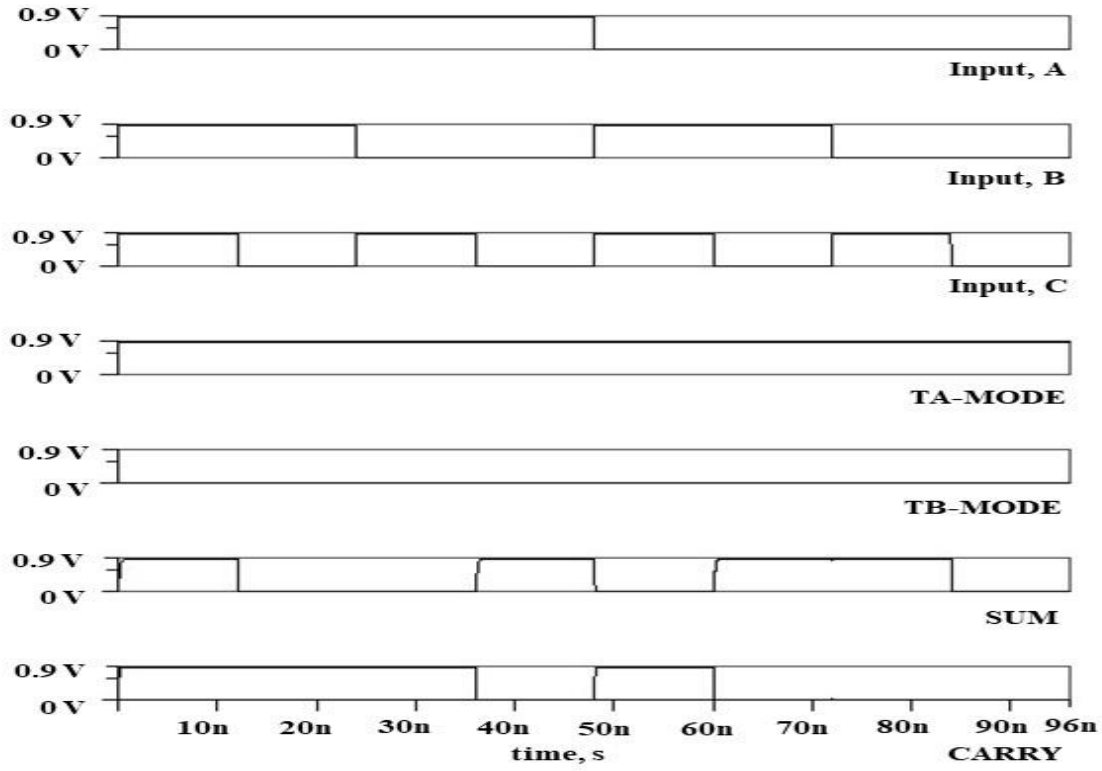



(b)

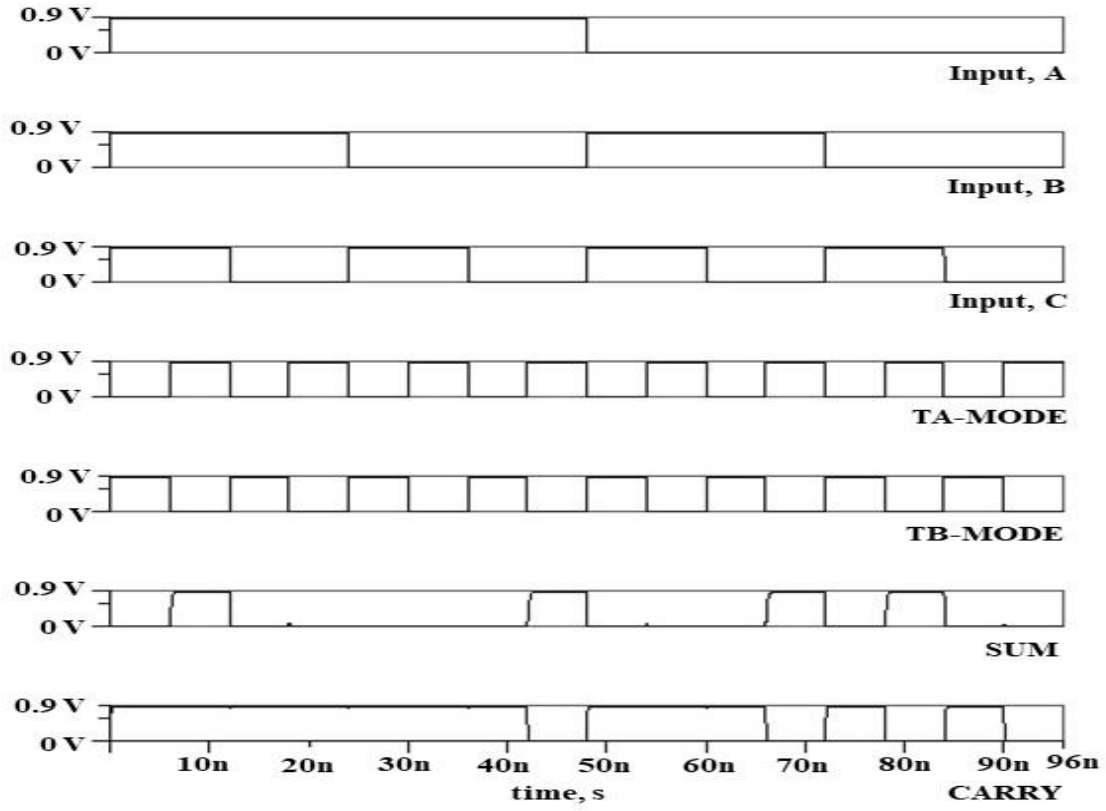
Fig. 5.8 Transient waveforms of proposed C-DML based 2-input gates at 32nm in dynamic mode (a) Type A (b) Type B

Further, in order to show the cascading of type A and type B topologies of proposed C-DML design, a 1-bit FA circuit is also implemented using the schematic shown in Fig. 3.5. The sum block is implemented using type B topology and the carry block is implemented using type A topology. The applied input waveforms for inputs A,B,C and MODE input for type A (TA-MODE) and type B topology (TB-MODE) are depicted in Fig. 5.9. The transient waveforms for sum (SUM) and carry (CARRY) in static mode is depicted in Fig. 5.9 (a). It may be noted that in static mode, the SUM bit is logic “1” when an odd number of logic “1” is present among the inputs and the CARRY bit is logic “1” when at least two of the three inputs are logic “1”.

The transient waveforms for sum (SUM) and carry (CARRY) in dynamic mode is depicted in Fig. 5.9 (b). In pre-charge/pre-discharge phase of dynamic mode, since the sum block is type B, therefore MODE is logic “1” causing the SUM bit to be at logic “0”. Similarly, since the carry block is type A therefore MODE is logic “0” as a result the CARRY bit is logic “1”. During the evaluation phase, the SUM bit becomes logic “1” when there's an odd number of logic “1” inputs, while the CARRY bit is logic “1” if at least two out of the three inputs are logic “1”.




(a)




(b)

Fig. 5.9 Transient waveforms of proposed C-DML based 1-bit FA (a) Static mode (b) Dynamic mode

#### 5.3.2.2 Performance comparison

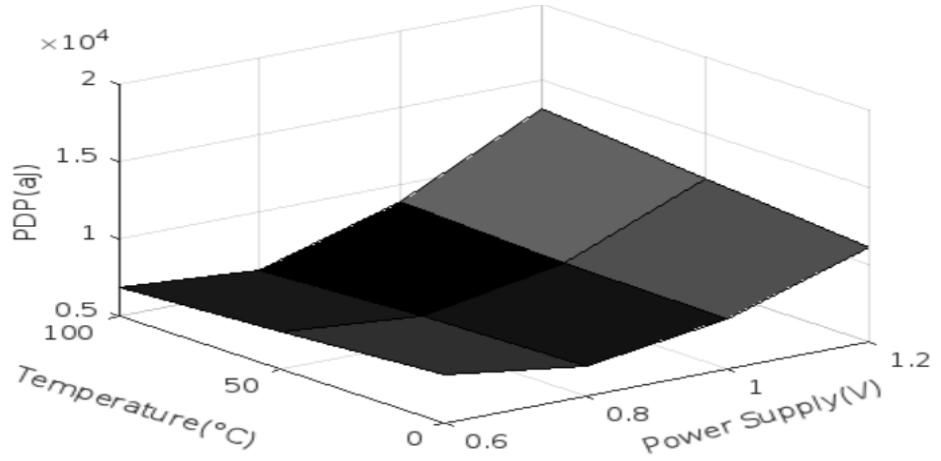
For comparison of performance of the considered designs in terms of power, delay and PDP, 2-input NAND, NOR, XOR gates and 1-bit FA circuit are simulated using HSPICE tool at 0.9 V supply voltage. Table 5.1 enlists the performance metrics i.e., power, delay and PDP of existing CMOS based footed DML and the proposed C-DML based circuits for type A and type B topologies in static and dynamic mode. Following are the observations made using Table 5.1:

i. For 2-input gates, a maximum PDP reduction of 69.81% and 79.73% is obtained using the proposed C-DML design for type A and type B topology respectively, as compared to its CMOS counterparts in static mode.
ii. In dynamic mode, the corresponding values are 63.43% and 76.89% for type A and type B topology respectively.
iii. For 1-bit FA circuit, PDP reduction of 60.61% is achieved using the proposed C-DML design as compared to its CMOS counterparts in static mode.
iv. In dynamic mode, a higher PDP reduction of 85.65% is obtained for 1-bit FA.

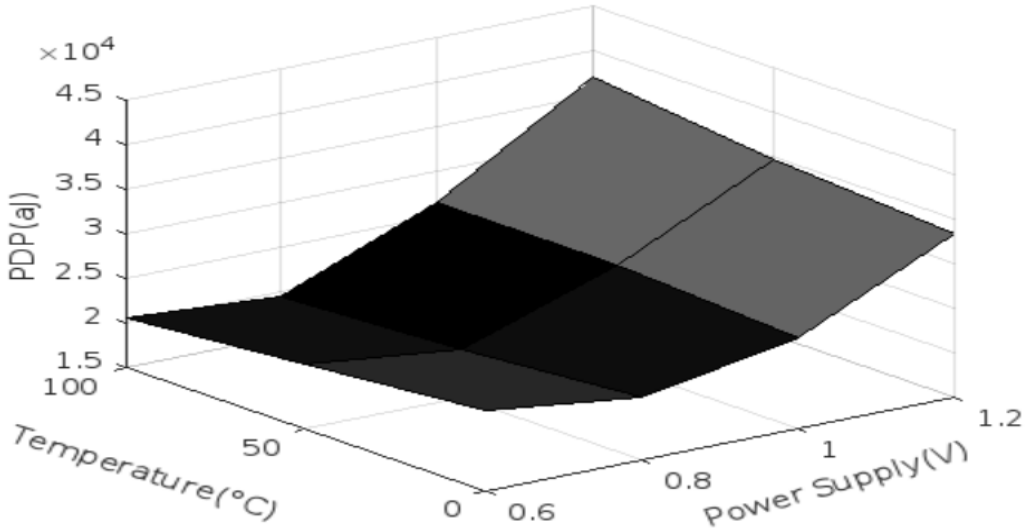
Table 5.1 Power, delay and PDP of proposed type A and type B C-DML based and CMOS footed DML based 2-input NAND, NOR, XOR gates and 1-bit FA circuit in static and dynamic mode at 32nm at 27℃

| Mode | Circuit | Power(uW) | | Delay(ps) | | PDP(aJ) | |
|---|---|---|---|---|---|---|---|
| Static | | CMOS Footed DML | C-DML | CMOS Footed DML | C-DML | CMOS Footed DML | C-DML |
| | TA-NAND2 | 0.856 | 0.812 | 155 | 67.1 | 132.68 | 54.49 |
| | TB-NAND2 | 0.848 | 0.803 | 221.8 | 71.8 | 188.09 | 57.66 |
| | TA-NOR2 | 0.829 | 0.781 | 225.3 | 72.2 | 186.77 | 56.39 |
| | TB-NOR2 | 0.824 | 0.713 | 298.8 | 70 | 246.21 | 49.91 |
| | TA-XOR2 | 1.335 | 1.022 | 347.3 | 139 | 463.65 | 142.06 |
| | TB-XOR2 | 1.291 | 0.876 | 391.9 | 128.7 | 505.94 | 112.74 |
| | FA | 11.51 | 9.061 | 655.1 | 327.8 | 7540.2 | 2970.2 |
| Dynamic | | | | | | | |
| | TA-NAND2 | 0.958 | 0.823 | 58.9 | 30.9 | 56.43 | 25.43 |
| | TB-NAND2 | 0.946 | 0.822 | 137.7 | 40.7 | 130.26 | 33.46 |
| | TA-NOR2 | 0.945 | 0.908 | 35.1 | 18.5 | 33.17 | 16.8 |
| | TB-NOR2 | 0.942 | 0.808 | 259.9 | 126.8 | 244.83 | 102.45 |
| | TA-XOR2 | 1.578 | 1.19 | 122.3 | 59.3 | 192.99 | 70.57 |
| | TB-XOR2 | 1.489 | 1.168 | 217.3 | 64 | 323.56 | 74.75 |
| | FA | 28.966 | 14.791 | 734.3 | 206.4 | 21269.73 | 3052.86 |

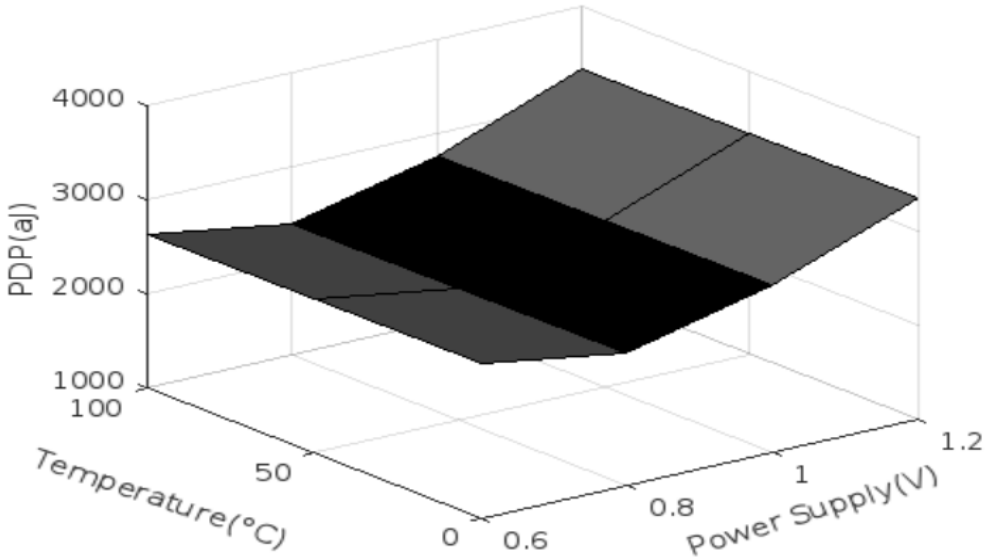
Further, the effect of temperature and voltage variations is thoroughly investigated by considering a 1-bit FA circuit to check the susceptibility of the proposed C-DML and CMOS based footed DML design to these variations. Figure 5.10 depicts the PDP variation with supply voltage and temperature for existing CMOS based footed DML design and the proposed C-DML design using a 1-bit FA circuit. As observed, the PDP variation of C-DML design to temperature variation is negligible as compared to its CMOS counterparts. The proposed design is capable of reducing PDP in static and dynamic mode even at different values of supply voltage and temperature.


×10^4
2
1.5
1
0.5
PDP(aJ)
100
50
0
Temperature(°C)
0.6
0.8
1
1.2
Power Supply(V)

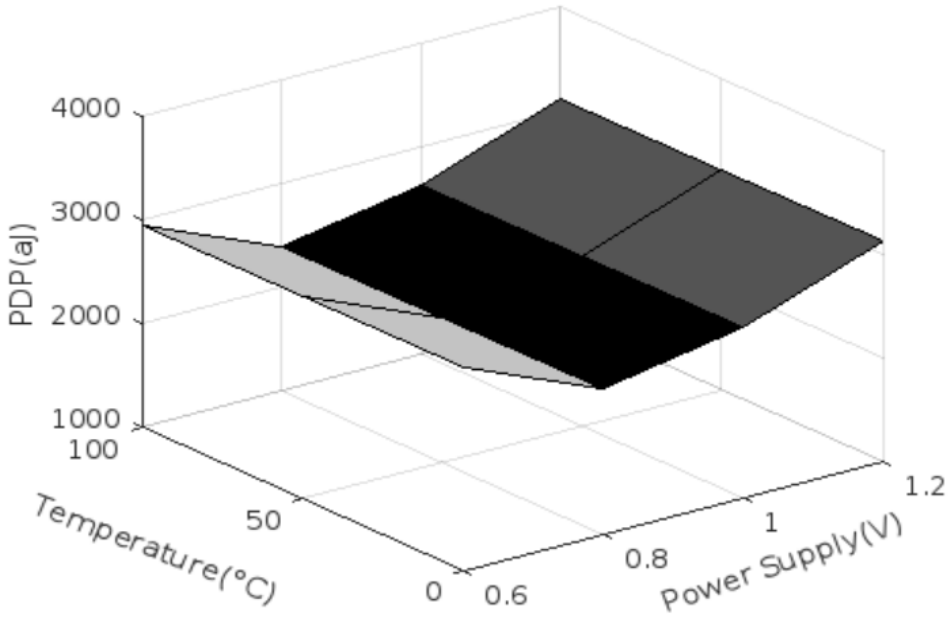
(a)


×10^4
4.5
4
3.5
3
2.5
2
1.5
PDP(aJ)
100
50
0
Temperature(°C)
0.6
0.8
1
1.2
Power Supply(V)

(b)


4000
3000
2000
1000
PDP(aJ)
100
50
0
Temperature(°C)
0.6
0.8
1
1.2
Power Supply(V)

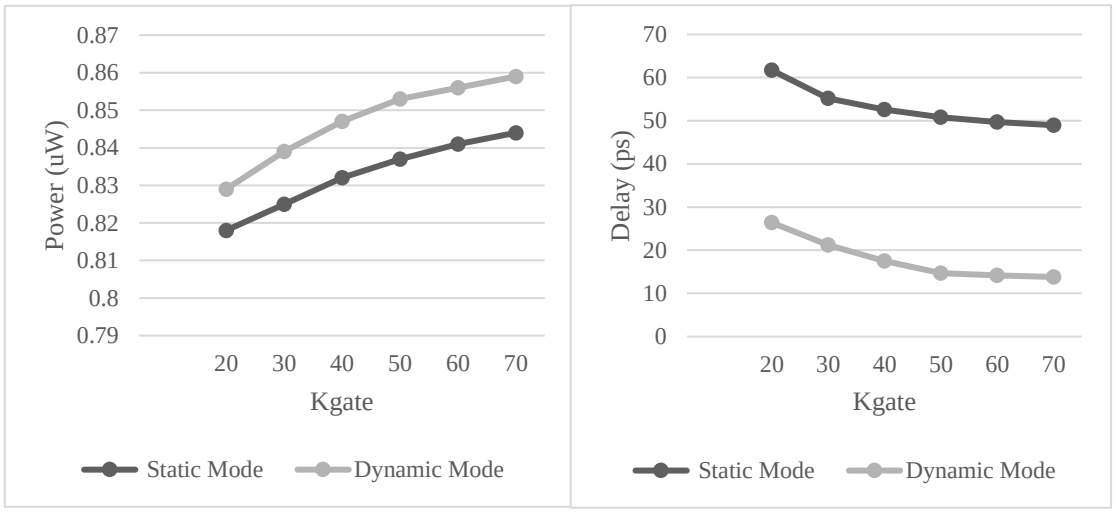
(c)




(d)

Fig. 5.10 Effect of temperature and voltage variations on the PDP of 1-bit FA circuit at 32nm (a) CMOS based footed DML design in static mode (b) CMOS based footed DML design in dynamic mode (c) Proposed C-DML design in static mode (d) Proposed C-DML design in dynamic mode

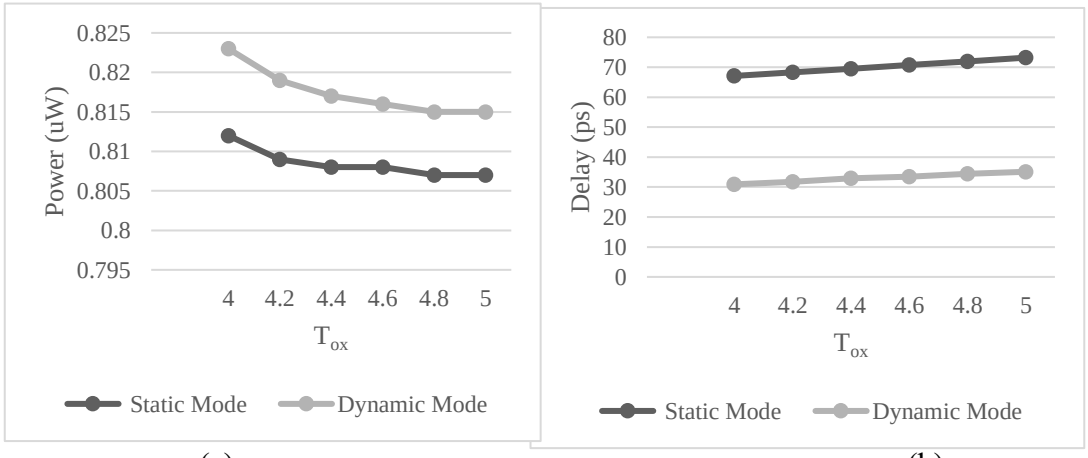
Moreover, an assessment of the impact of variation of oxide thickness ($T_{OX}$), dielectric constant (Kgate) and chiral indices on power and delay of the proposed C-DML design is conducted, utilizing a 2-input type A NAND gate in both static and dynamic mode. The effect of variation of dielectric constant (Kgate) for proposed type A C-DML based 2-input NAND gate in static and dynamic mode on power and delay is shown in Fig. 5.11. It can be observed that the power increases when the dielectric constant goes up, due to lowering of the threshold voltage. The CNTFET with higher dielectric constant switches on quicker than one with lower dielectric constant due to reduced threshold voltage. Consequently, the delay of the proposed design decreases as dielectric constant increases in both static and dynamic mode.




(a) (b)

Fig. 5.11 Effect of variation of dielectric constant (Kgate) for proposed type A C-DML based 2-input NAND gate in static and dynamic mode on (a) Power (b) Delay

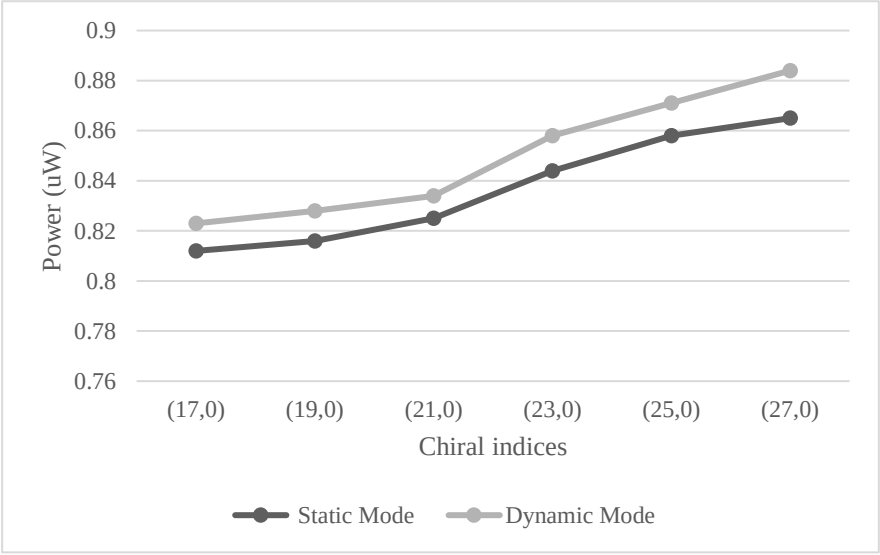
The effect of the variation of oxide thickness ($T_{OX}$) on power and delay in the proposed type A C-DML based 2-input NAND gate in static and dynamic mode is depicted in Fig. 5.12. Increasing oxide thickness in CNTFETs raises the threshold voltage due to heightened capacitance between the gate and the channel. This results in reduced power but increased delay in the proposed design as oxide thickness increases in both static and dynamic mode.



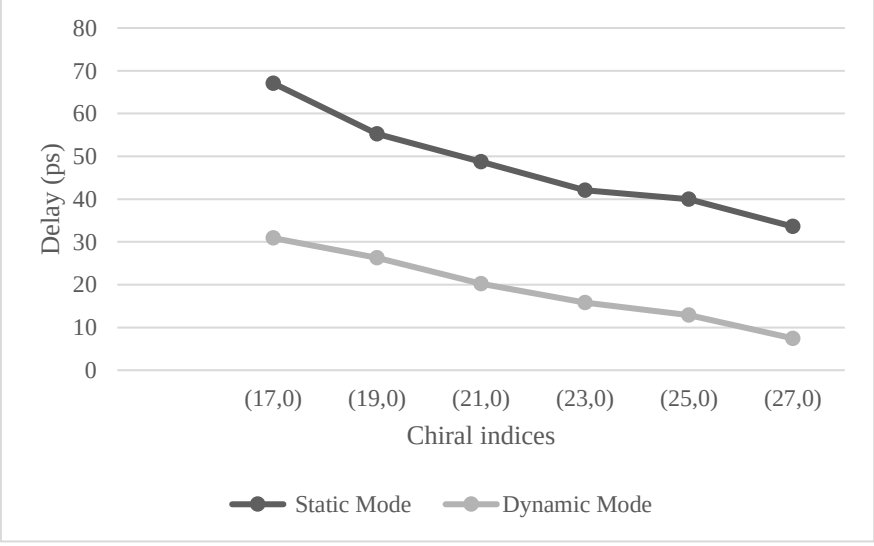

(a) (b)

Fig. 5.12 Effect of variation of oxide thickness ($T_{OX}$) for proposed type A C-DML based 2-input NAND gate in static and dynamic mode on (a) Power (b) Delay

Further, effect of variation of chiral indices for proposed type A C-DML based 2-input NAND gate in static and dynamic mode on power and delay is shown in Fig. 5.13. As the chiral indices value increases, the threshold voltage of CNTFETs decreases. As a result, the power of the proposed design increases and the corresponding delay value decreases in both static and dynamic mode.




(a)




(b)

Fig. 5.13 Effect of variation of chiral indices for proposed type A C-DML based 2-input NAND gate in static and dynamic mode on (a) Power (b) Delay

## 5.4 Proposed Design-VI: CNTFET based M-DMTGDI (C-MDMTGDI)

The dual-mode functionality was incorporated into the MOSFET based TGDI design to create DMTGDI design, as already discussed in preceding chapters. Analogously, this section leverages the benefits of CNTFETs and introduces the CNTFET based DMTGDI, known as C-DMTGDI. To tackle contention issues in the MOSFET based DMTGDI design, the M-DMTGDI design was introduced as a solution. A similar issue persists in the C-DMTGDI design. Hence, proposed design-VI i.e. CNTFET based M-DMTGDI design, denoted as C-MDMTGDI, has been put forward in this section.

### 5.4.1 Operation

The schematic of proposed C-MDMTGDI cell is shown in Fig. 5.14. A type A inverter in footed C-DML configuration is added to the output node of CNTFET based TGDI (C-TGDI) cell to get the proposed C-MDMTGDI cell. It can operate in static and dynamic mode. In static mode, transistor $C_1$ is off and footer transistor $C_3$ is on as MODE input is constant logic "1". The circuit works in static mode by generating an output in accordance with the logic that the C-TGDI block has implemented. When operating in dynamic mode, the MODE input is a clock signal that enables pre-charge and evaluation phases of operation. The output is pre-charged to $V_{DD}$ in pre-charge phase (MODE=logic "0"), and the output is evaluated in the evaluation phase (MODE= logic "1") in accordance with the implemented logic function.

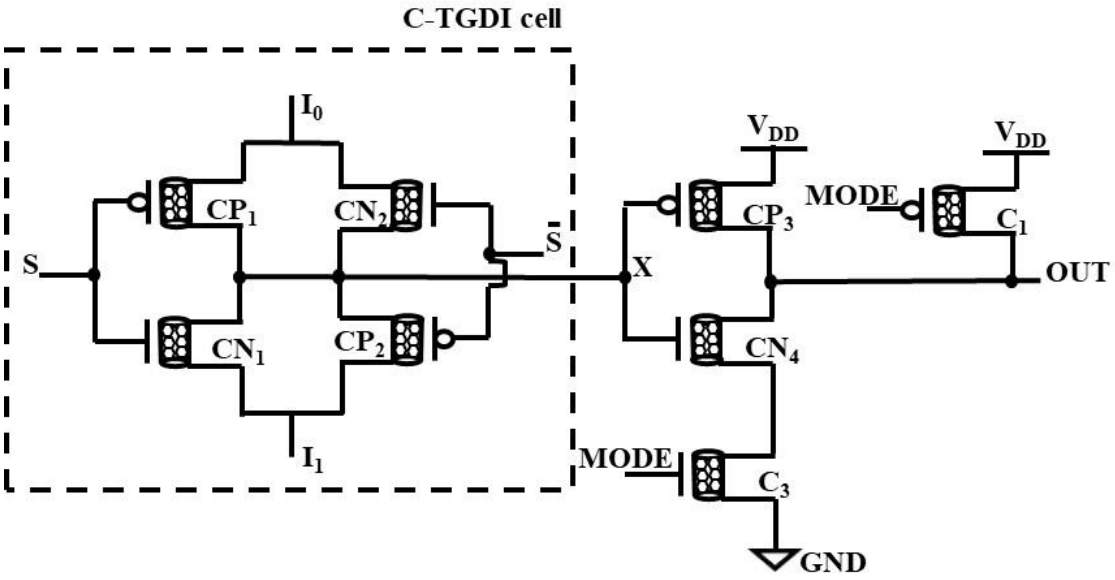
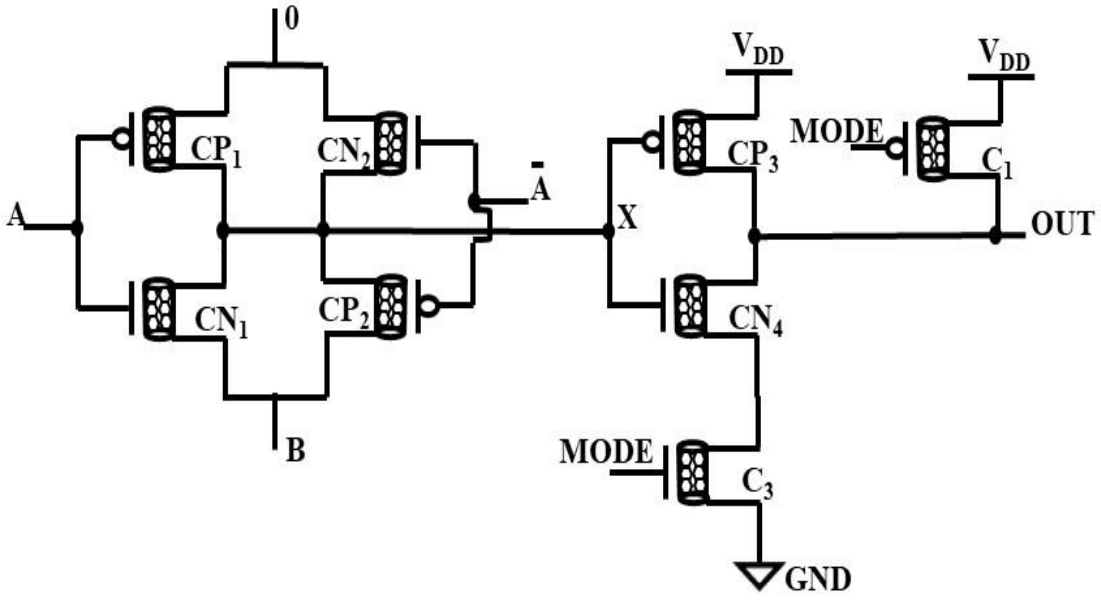



Fig. 5.14 Proposed C-MDMTGDI cell

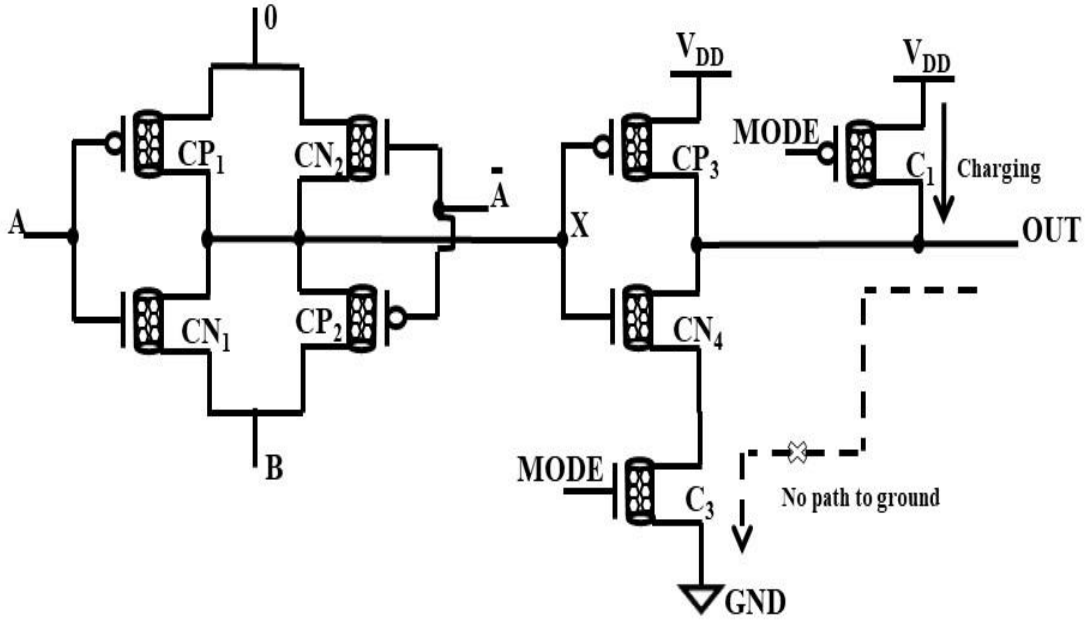
A two-input NAND gate based on the proposed C-MDMTGDI cell is illustrated in Fig. 5.15 (a). The output at node 'X' corresponds to the logical AND function of inputs (A, B). In the static mode, the MODE input is logic “1”, causing transistor $C_1$ to be in the off state while keeping the footer transistor $C_3$ on. It may be noted that output for NAND gate is logic “1” when any of the inputs is logic “0” Thus, the overall functionality will be NAND gate and output is determined by the inputs applied to the gate.

In the dynamic mode, the circuit operates in two phases: pre-charge and evaluation, with a clock signal applied as the MODE input. During the pre-charge phase, when MODE is logic “0”, transistor $C_1$ becomes on and charges the output node, OUT, to $V_{DD}$, as shown in Fig. 5.15 (b). The footer transistor $C_3$ is off, preventing any discharge of the output node. Therefore, there is no contention at the output node due to the presence of the footer transistor $C_3$, ensuring that the proposed design yields the desired output voltage. In the evaluation phase, transistor $C_1$ is off, and the footer transistor $C_3$ is on, leading to the evaluation of the output based on the applied inputs. It may be noted that output for NAND gate is logic “1” when any of the inputs is logic “0” in evaluation phase. Thus,

C-MDMTGDI design can operate in both static and dynamic mode without any contention at the output node.




(a)




(b)

Fig. 5.15 Proposed C-MDMTGDI design (a) 2-input NAND gate (b) pre-charge phase of dynamic mode with no contention

### 5.4.2 Simulation results

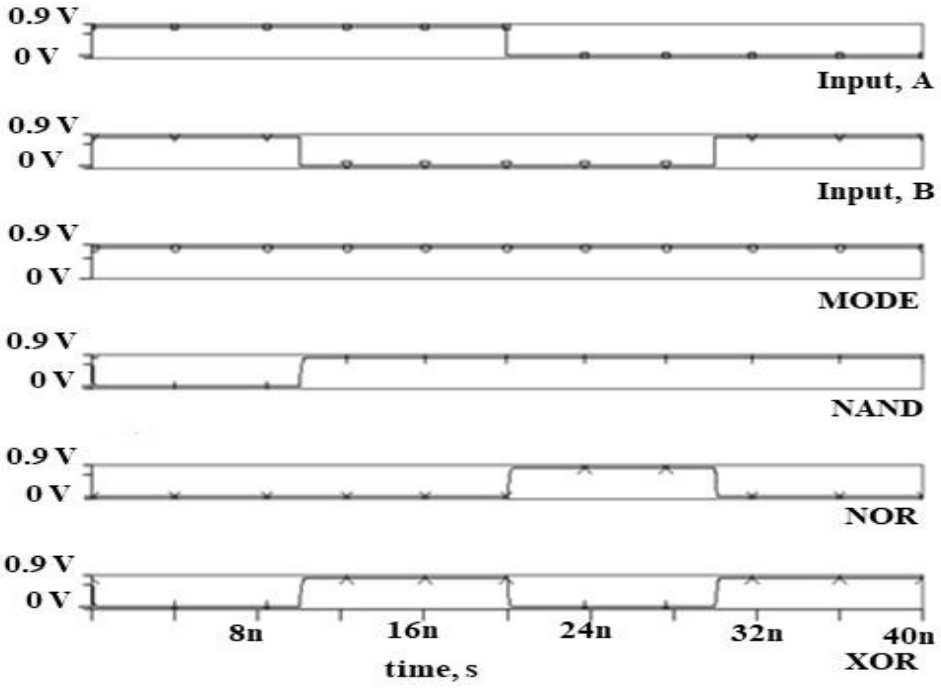
This section consists of two subsections namely functional verification to examine the working of the proposed design. A performance comparison is carried out in terms of power, delay, and PDP. The proposed C-MDMTGDI design is compared with C-DMTGDI design in CNTFET as well as CMOS domain for 2-input NAND, NOR, XOR gates and 1-bit FA circuit. The simulations are carried out using HSPICE tool with 32nm CNTFET Stanford model and 32nm BSIM4 model card for bulk CMOS at 0.9V supply voltage and a load capacitance of 5fF. The proposed design is implemented using a chiral indices of (17,0).

#### 5.4.2.1 Functional verification

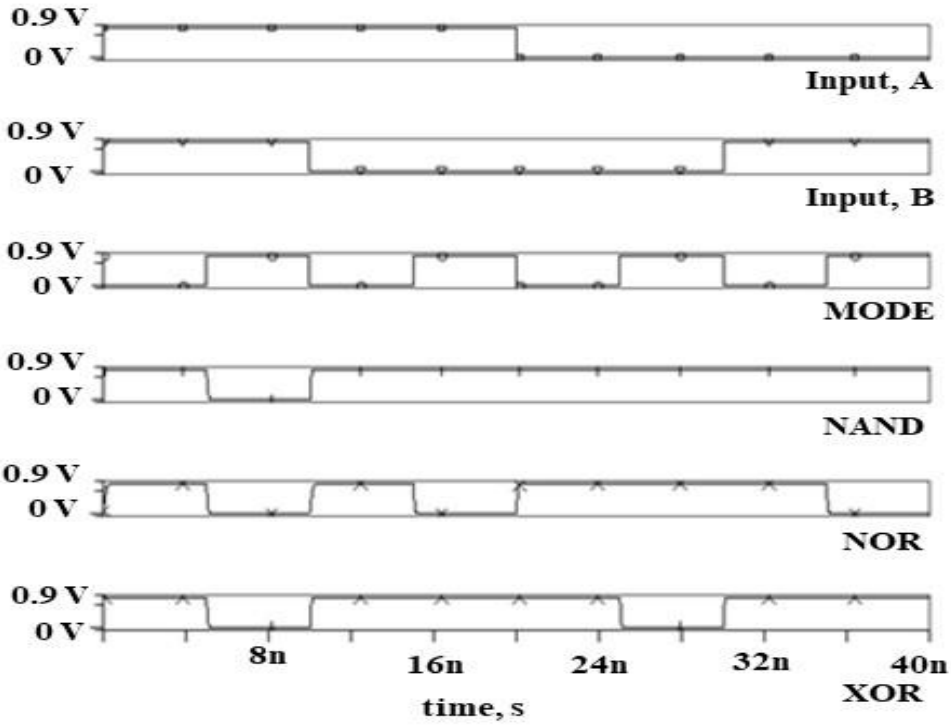
Figure 5.16 displays the transient waveforms of 2-input gates, namely NAND, NOR, and XOR gates, which have been implemented using the proposed C-MDMTGDI design. The waveforms are presented for both static mode (Fig. 5.16 (a)) and dynamic mode (Fig. 5.16 (b)). In static mode, an output of logic “1” is generated by a NAND gate if logic “0” is present in any of its inputs, and an output of logic “0” is yielded by a NOR gate if logic “1” is present in any of its inputs. For XOR gate, the output is logic “1” when there is an odd number of logic “1” inputs otherwise, the output is logic “0”. Hence, the simulated values match with the theoretical values.

In dynamic mode, the MODE input is supplied with a clock signal having two phases of operation- pre-charge and evaluation. During the pre-charge phase, the MODE input is logic “0”, resulting in the charging of the output to the supply voltage for all gates. Conversely, in the evaluation phase, the MODE input is logic “1”. A NAND gate produces an output of logic “1” if any of its inputs are logic “0”, while a NOR gate produces an output of logic “0” if any of its inputs are logic “1”. For XOR gate, the output is logic “1” when there is an odd number of logic “1” inputs otherwise, the output is logic “0”.

Therefore, the proposed C-MDMTGDI based NAND, NOR, and XOR gates operate correctly in dynamic mode



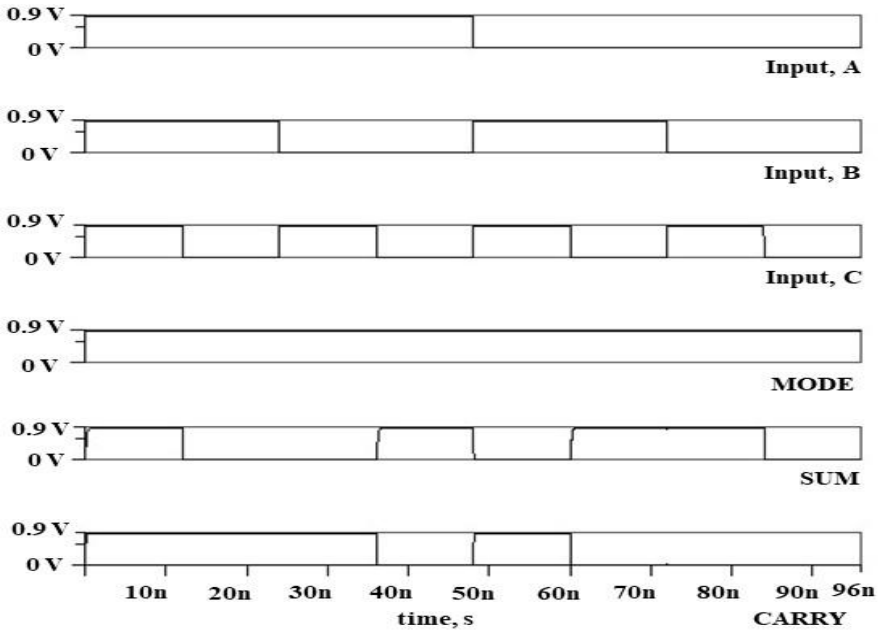

(a)



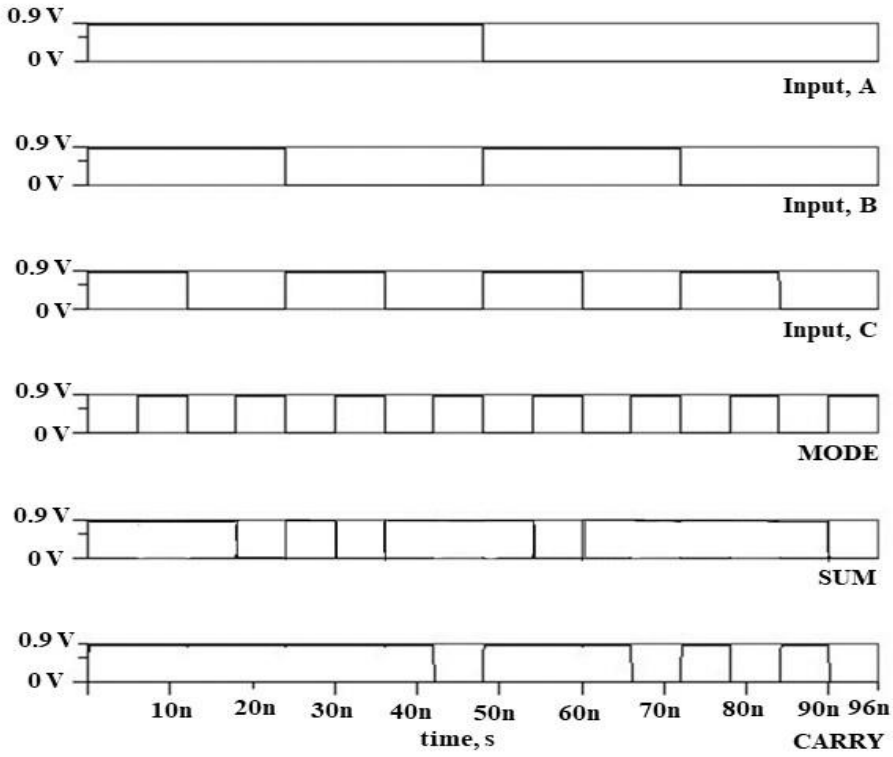

(b)

Fig. 5.16 Transient waveforms of proposed C-MDMTGDI design for 2-input gates (a) Static mode (b) Dynamic mode

A 1-bit FA circuit is also implemented using the proposed C-MDMTGDI design. The SUM block generates SUM bit which is generated by using two C-TGDI based XNOR gates, as given in Table 2.1, followed by a footed C-DML inverter. A two-stage network (CARRY block) is used to generate the CARRY bit where first stage consists of three C-TGDI based NAND gates and the second stage consists of a C-TGDI based AND gate, followed by a footed C-DML inverter The applied input waveforms for inputs A,B,C and MODE input (MODE) are depicted in Fig. 5.17. The transient waveforms for sum (SUM) and carry (CARRY) are depicted in Fig. 5.17 (a) and Fig. 5.17 (b) for static and dynamic mode respectively. It may be noted that in static mode, the SUM bit is logic "1" when an odd number of logic "1" among the inputs and the CARRY bit is logic "1" when at least two of the three inputs are logic "1". In pre-charge/pre-discharge phase of dynamic mode, the SUM and CARRY bit are logic "1" as MODE input is logic "0". During the evaluation phase, the SUM bit becomes logic "1" when there's an odd number of logic "1" inputs, while the CARRY bit is logic "1" if at least two out of the three inputs are logic "1".




(a)




(b)

Fig. 5.17 Transient waveforms of proposed C-MDMTGDI based 1-bit FA (a) Static mode (b) Dynamic mode

### 5.4.2.2 Performance comparison

To ensure a fair comparison, CMOS based DMTGDI and M-DMTGDI designs, as well as CNTFET based DMTGDI designs, are implemented alongside the proposed C-MDMTGDI design. The CNTFET-based DMTGDI design is denoted as C-DMTGDI, and the C-DMTGDI cell is depicted in Fig. 5.18. The performance of the existing and proposed designs is compared in terms of power, delay and PDP using 2-input NAND, NOR, XOR gates and 1-bit FA circuit. All the circuits are simulated using HSPICE tool at 0.9 V supply voltage.

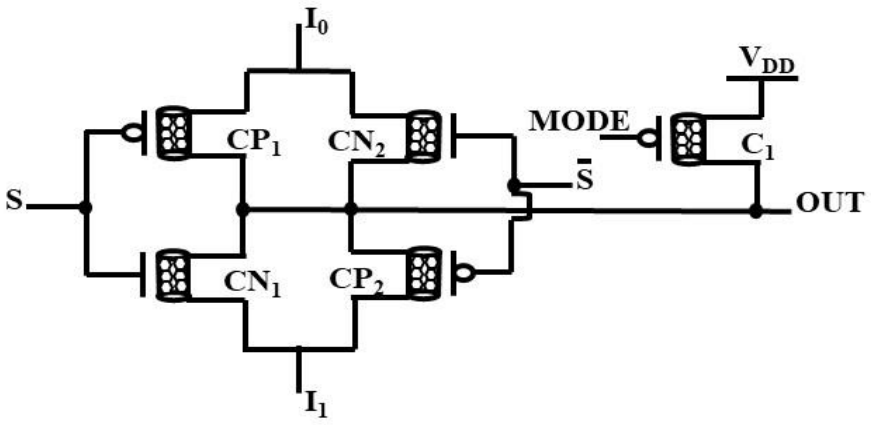



Fig. 5.18 C-DMTGDI cell

Table 5.2 enlists the performance metrics i.e., power, delay and PDP of CMOS based DMTGDI, CMOS based M-DMTGDI, C-DMTGDI and C-MDMTGDI design in static and dynamic mode. The observations from Table 5.2 is as follows:

i. For 2-input gates, the proposed C-MDMTGDI offers a maximum % PDP reduction of 97.85% and 93.82% as compared to its CMOS counterparts in static and dynamic mode respectively.

ii. For 1-bit FA circuit, the corresponding values are 87.71% and 89.21%.

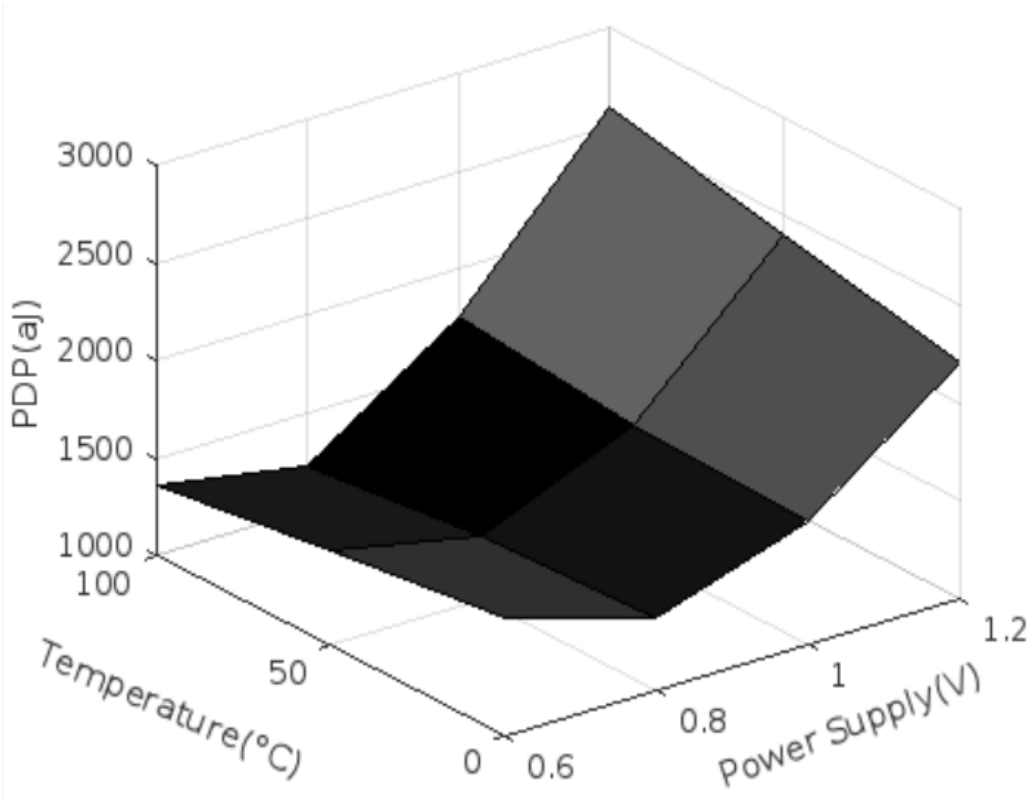
iii. In contrast to C-DMTGDI design, PDP of proposed C-MDMTGDI design deteriorates in static mode. However, in dynamic mode, there is a significant improvement in PDP of the proposed design.

iv. Consequently, operating the proposed C-MDMTGDI design in dynamic mode for over 50% longer duration than in static mode demonstrates significantly enhanced efficiency at PDP reduction compared to prolonged operation in static mode.

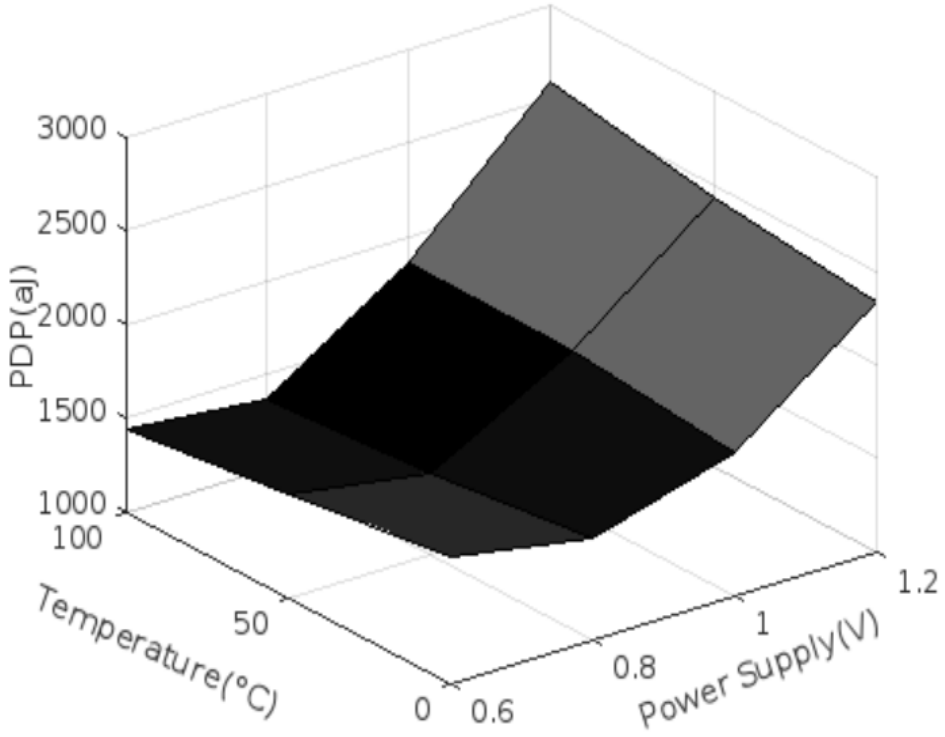
Table 5.2 Power, delay and PDP of existing CMOS based DMTGDI, CMOS based M-DMTGDI, proposed C-DMTGDI and C-MDMTGDI based 2-input NAND, NOR, XOR gates and 1-bit FA circuit in static and dynamic mode at 27℃

| Mode | Circuit | Power(uW) | | | | Delay(ps) | | | | PDP(aJ) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Static | | CMOS DMTGDI | C-DMTGDI | CMOS MDMTGDI | C-MDMTGDI | CMOS DMTGDI | C-DMTGDI | CMOS MDMTGDI | C-MDMTGDI | CMOS DMTGDI | C-DMTGDI | CMOS MDMTGDI | C-MDMTGDI |
| | NAND | 1.36 | 1.25 | 1.64 | 1.18 | 72 | 16.2 | 158.6 | 33 | 97.92 | 20.25 | 260.1 | 38.94 |
| | NOR | 0.95 | 0.81 | 1.12 | 0.69 | 47.9 | 16 | 146.4 | 32.6 | 45.51 | 12.96 | 163.97 | 22.49 |
| | XOR | 4.51 | 0.46 | 4.12 | 0.48 | 70.4 | 16.2 | 149.8 | 27.7 | 317.5 | 7.45 | 617.18 | 13.29 |
| | FA | 3.4 | 1.8 | 8.04 | 3.9 | 100.8 | 18.79 | 185.56 | 46.98 | 342.72 | 33.82 | 1491.18 | 183.22 |
| Dynamic | | | | | | | | | | | | | |
| | NAND | 139.6 | 41.8 | 4.65 | 1.2 | 13.8 | 5.99 | 47.3 | 20.3 | 1926.48 | 250.38 | 219.95 | 24.36 |
| | NOR | 290.7 | 70.18 | 5.36 | 1.19 | 18 | 6.9 | 39.8 | 19.9 | 5232.6 | 484.24 | 213.33 | 23.68 |
| | XOR | 295.5 | 61.6 | 4.07 | 0.66 | 11.7 | 5.3 | 43.8 | 16.7 | 3457.35 | 326.48 | 178.27 | 11.02 |
| | FA | 4048.4 | 807.65 | 28.83 | 7.32 | 38.64 | 10.26 | 52.03 | 22.11 | 156430.18 | 8286.49 | 1500.02 | 161.85 |

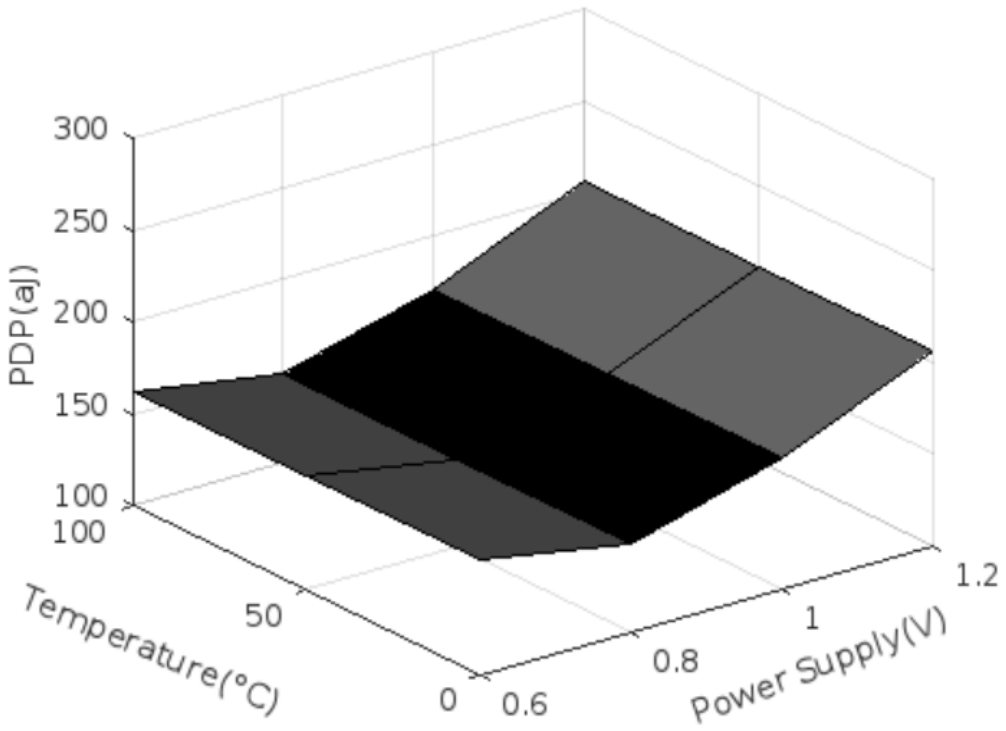
Furthermore, a comprehensive examination of the impact of temperature and voltage variations is conducted, employing a 1-bit FA circuit to assess the vulnerability of the proposed C-MDMTGDI and CMOS based M-DMTGDI design to these variations. In Fig. 5.19, the PDP for both C-MDMTGDI and CMOS based M-DMTGDI is illustrated across various supply voltages and temperatures. Notably, the PDP of the CNTFET exhibits minimal variation in response to temperature fluctuations. In contrast, the CMOS based MDMTGDI is more susceptible to changes in temperature and voltage. The proposed design demonstrates its capability to reduce PDP in both static and dynamic mode across various supply voltages and temperatures.



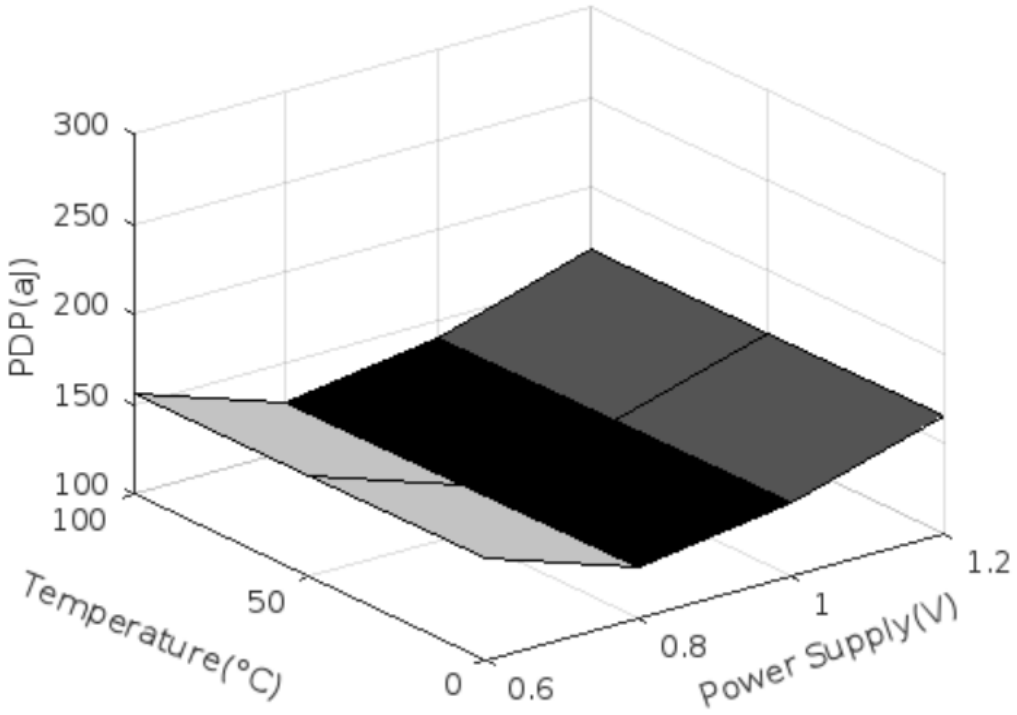

(a)


3000
2500
2000
1500
1000
PDP(aJ)
100
50
0
Temperature(°C)
0.6
0.8
1
1.2
Power Supply(V)

(b)


300
250
200
150
100
PDP(aJ)
100
50
0
Temperature(°C)
0.6
0.8
1
1.2
Power Supply(V)

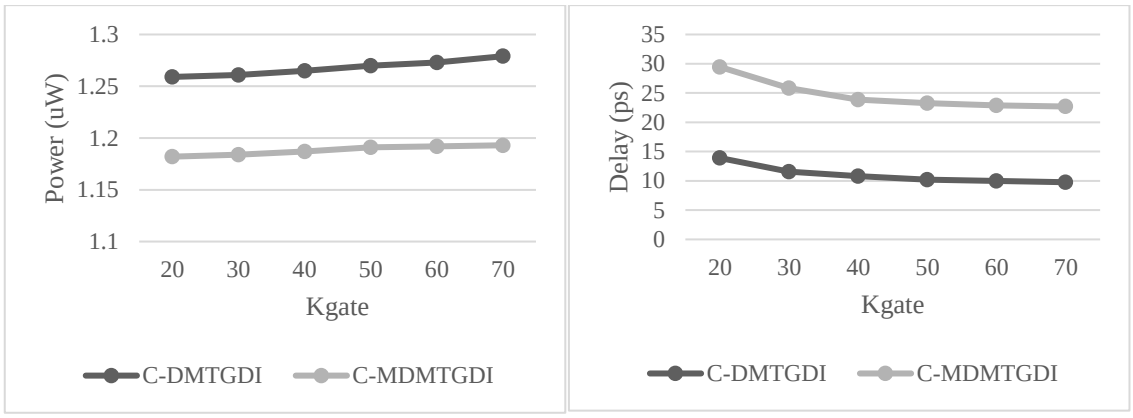
(c)




(d)

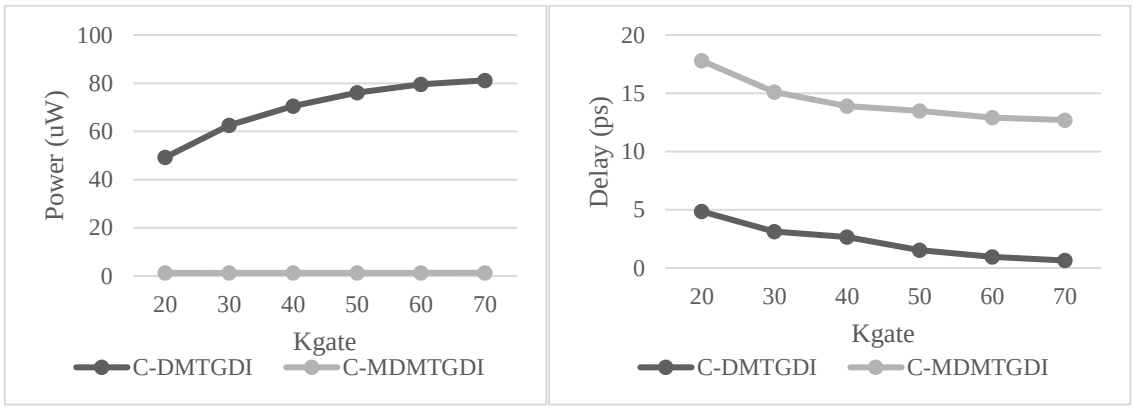
Fig. 5.19 Effect of temperature and voltage variations on the PDP of 1-bit FA circuit at 32nm (a) CMOS based M-DMTGDI design in static mode (b) CMOS based M-DMTGDI design in dynamic mode (c) Proposed C-MDMTGDI design in static mode (d) Proposed C-MDMTGDI design in dynamic mode

Further, an assessment is performed to analyse how changes in oxide thickness, dielectric constant, and chiral indices affect the power and delay of the proposed C-MDMTGDI and C-DMTGDI design, using a 2-input NAND gate in both static and dynamic mode. In Fig. 5.20 and Fig. 5.21, the impact of changing dielectric constant (Kgate) on power and delay for the proposed C-MDMTGDI and C-DMTGDI based 2-input NAND gate in static and dynamic mode is presented respectively. It can be observed that an increase in dielectric constant results in increased power and decreased delay for the proposed design due to reduced threshold voltage in both static and dynamic mode.




(a) (b)

Fig. 5.20 Effect of variation of dielectric constant (Kgate) for proposed C-MDMTGDI and C-DMTGDI based 2-input NAND gate in static mode on (a) Power (b) Delay

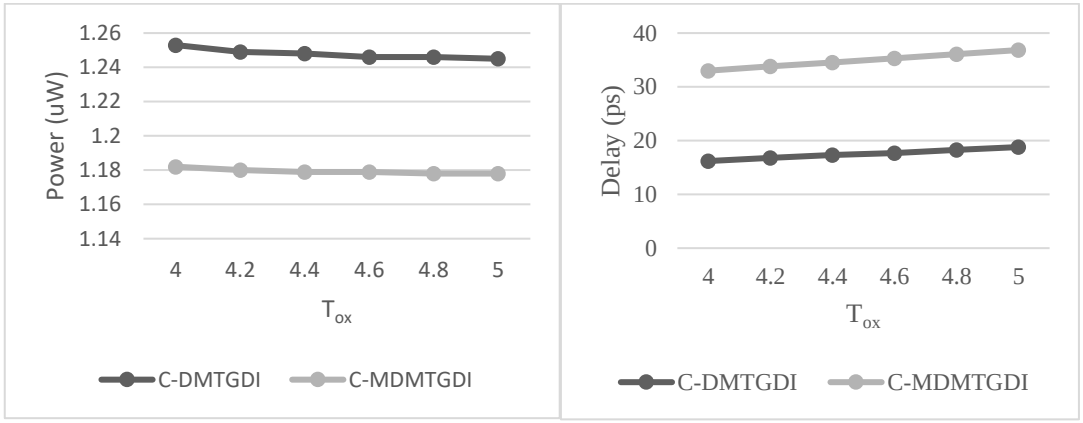



(a) (b)

Fig. 5.21 Effect of variation of dielectric constant (Kgate) for proposed C-MDMTGDI and C-DMTGDI based 2-input NAND gate in dynamic mode on (a) Power (b) Delay

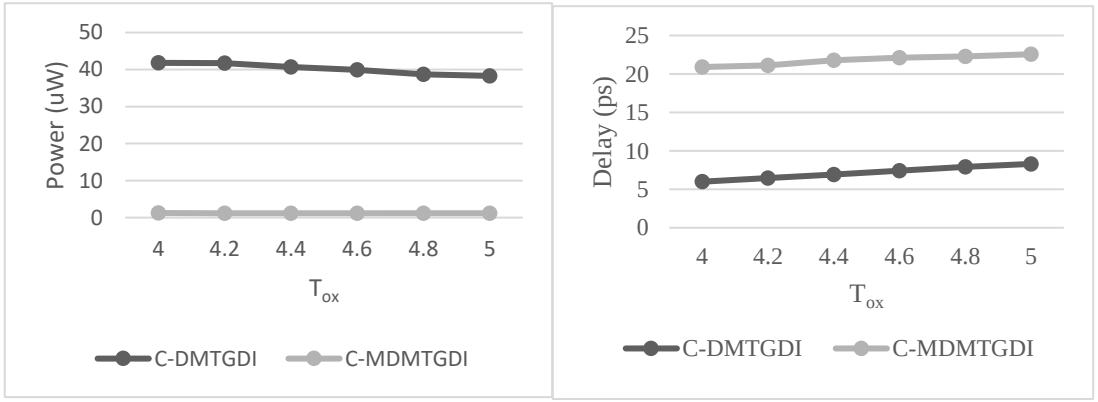
Figure 5.22 and Figure 5.23 demonstrate the impact of changing oxide thickness ($T_{ox}$) on power and delay for the proposed C-MDMTGDI and C-DMTGDI based 2-input NAND gate in static and dynamic mode respectively. It is evident that increasing oxide thickness ($T_{ox}$) leads to decreased power and increased delay in the proposed design in

both static and dynamic mode. This is because increasing oxide thickness raises the threshold voltage in CNTFETs due to increased gate-channel capacitance.




(a) (b)

Fig. 5.22 Effect of variation of oxide thickness ($T_{OX}$) for proposed C-MDMTGDI and C-DMTGDI based 2-input NAND gate in static mode on (a) Power (b) Delay

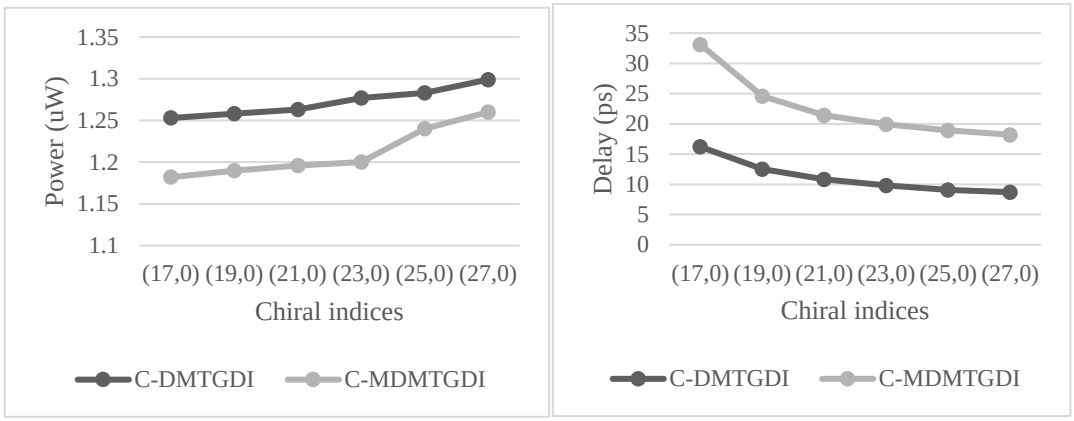



(a) (b)

Fig. 5.23 Effect of variation of oxide thickness ($T_{OX}$) for proposed C-MDMTGDI and C-DMTGDI based 2-input NAND gate in dynamic mode on (a) Power (b) Delay

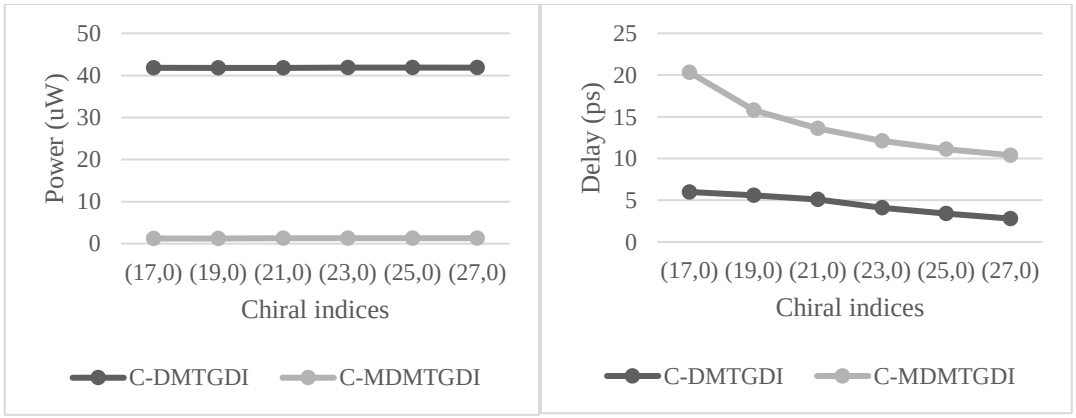
The impact of changing chiral indices on power and delay for the proposed C-MDMTGDI and C-DMTGDI based 2-input NAND gate in static and dynamic mode is depicted in Fig. 5.24 and Fig. 5.25, respectively. It can be seen that as chiral indices increase, due to a decrease in the threshold voltage of CNTFETs, the power of the

proposed design increases while the delay value decreases in both static and dynamic mode.




(a) (b)

Fig. 5.24 Effect of variation of chiral indices for proposed C-MDMTGDI and C-DMTGDI based 2-input NAND gate in static mode on (a) Power (b) Delay




(a) (b)

Fig. 5.25 Effect of variation of chiral indices for proposed C-MDMTGDI and C-DMTGDI based 2-input NAND gate in dynamic mode on (a) Power (b) Delay

## 5.5 Proposed Design-VII: LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI

This section investigates the leakage mechanism in proposed C-MDMTGDI design. Further, three leakage reduction techniques, namely LECTOR, GALEOR, and

LCNT, are incorporated in the proposed C-MDMTGDI design, referred to as LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI design respectively.

### 5.5.1 Operation

To understand the leakage mechanism in C-MDMTGDI design, consider a C-MDMTGDI based 2-input NAND gate, shown in Fig. 5.15 (a). In static mode, the pre-charge transistor ($C_1$) in the proposed C-MDMTGDI NAND gate is turned off . There is some leakage current in the off transistors as well as the off pre-charge transistor ($C_1$), depending on the inputs applied. A path for a current to pass from the supply voltage to ground is thus created. Similar to this, in pre-charge phase of dynamic mode, transistor $C_1$ is utilised to charge the output to supply voltage. Since transistor $C_3$ is off in pre-charge phase, the PDN should ideally have no current flowing through it. However, leakage current flows through off transistors appearing in path between supply voltage and ground. In evaluation phase, leakage current exists in off transistors and is controlled by the applied inputs.

The working of proposed LECTOR based, GALEOR based and LCNT based C-MDMTGDI design is elucidated as follows. The proposed LECTOR based C-MDMTGDI design incorporates LCTs between PUN and PDN of output inverter of C-MDMTGDI design for leakage reduction, as illustrated in Fig. 5.26. Consider the working of LECTOR based C-MDMTGDI 2-input NAND gate, transistor $LCT_1$ (P-CNTFET) and $LCT_2$ (N-CNTFET) are introduced between the PUN and PDN. The drain nodes of $LCT_1$ and $LCT_2$ are connected to form the output node to which the pre-charge transistor $C_1$ is connected. In static mode, the MODE input is constant logic “1” making transistor $C_1$ off. This MODE input would also turn on transistor $C_3$. The output in this case depends on the inputs applied at input terminals of NAND gate. When

(A,B)=(1,1), node X is charged to logic "1". As a result, transistor $CP_3$ is off and $CN_4$ is on, $LCT_2$ would be in cut-off in this case. The effective resistance is increased from supply voltage to ground path due to the presence of LCTs. The analysis can be carried out similarly for all other input combinations in static mode.

In pre-charge phase of dynamic mode, transistor $C_1$ charges the output node to $V_{DD}$ as MODE= logic "0". In evaluation phase, MODE= logic "1", transistor $C_1$ is off and footer transistor $C_3$ is on. According to the inputs applied, output is calculated. Due to the presence of off LCT transistor $LCT_2$, flow of leakage current is restricted and leakage is reduced. The analysis can be carried out similarly for all other input combinations in evaluation phase.

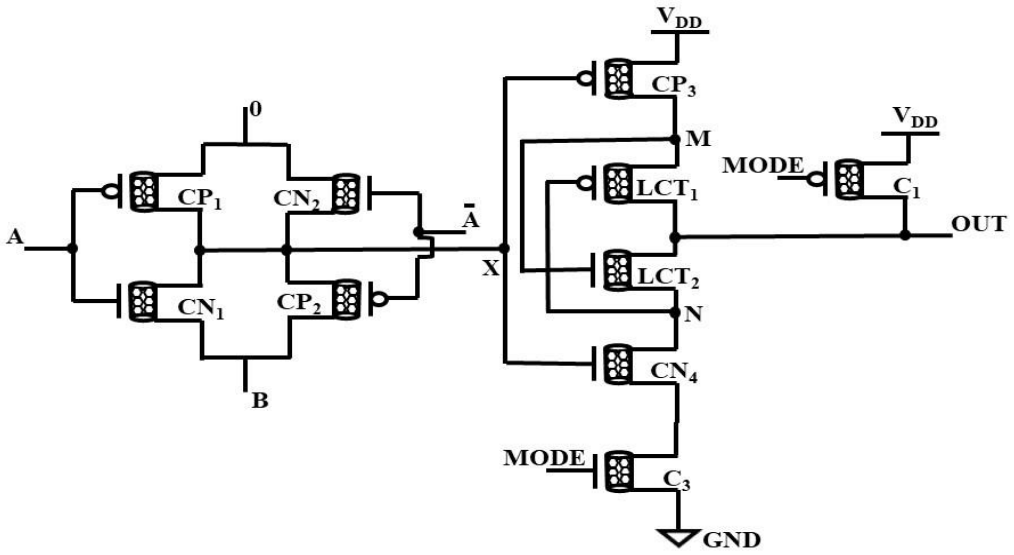



Fig. 5.26 Proposed LECTOR based C-MDMTGDI 2-input NAND gate

Another proposed approach for leakage reduction is incorporation of GLTs in the C-MDMTGDI design. Figure 5.27 illustrates a typical GALEOR based C-MDMTGDI NAND gate. The GLTs are inserted between PUN and PDN of output inverter. The gate and drain terminal of $GLT_1$ and $GLT_2$ are interconnected. The common source of $GLT_1$ and $GLT_2$ is used to get the output, OUT to which the transistor $C_1$ is connected. In static mode (MODE= logic "1"), transistor $C_1$ is off and footer transistor $C_3$ is on. $GLT_1$ and

$GLT_2$ switching is governed by voltages at node M and N. When (A,B)=(1,1), a direct path is established between node X and $V_{DD}$ which makes node X as logic "1", transistor $CP_3$ is off and $CN_4$ is on. Transistor $GLT_1$ is off, due to which the resistance of path from supply voltage to ground increases, which eventually reduces leakage. The analysis can be carried out similarly for all other input combinations. During pre-charge phase (MODE=logic "0"), transistor $C_1$ charges the output node to supply voltage, here the leakage current is governed by applied inputs. In evaluation phase (MODE= logic "1"), with (A,B) = (1,1), node X is connected to $V_{DD}$, transistor $GLT_1$ is off, which reduces the leakage current. The analysis can be carried out similarly for all other input combinations in evaluation phase.

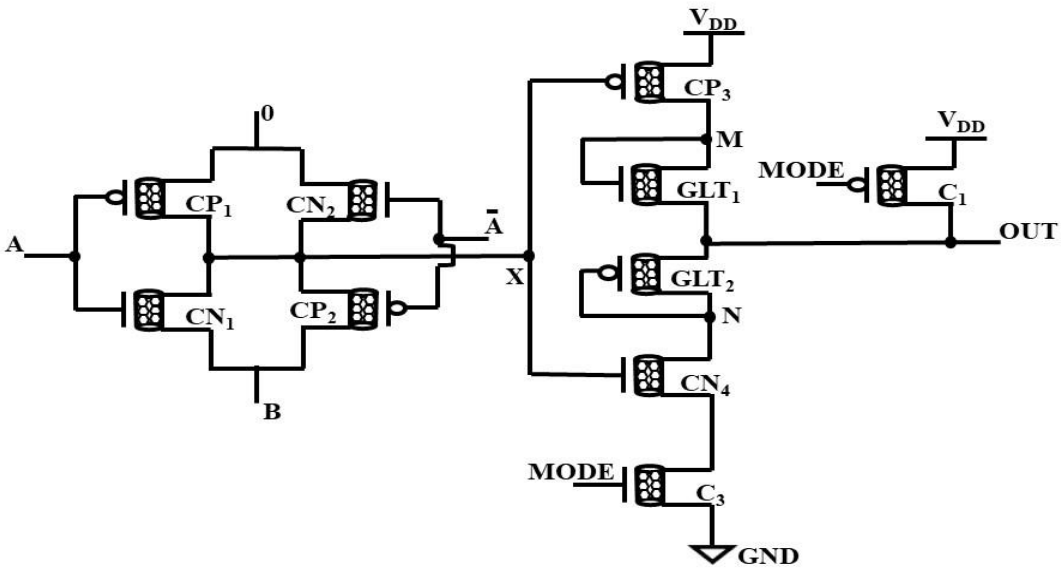



Fig. 5.27 Proposed GALEOR based C-MDMTGDI 2-input NAND gate

The third proposed approach for leakage reduction in C-MDMTGDI design is by introducing LCNTs between PUN and PDN of the output inverter of C-MDMTGDI design. A LCNT based C-MDMTGDI based 2-input NAND gate is depicted in Fig. 5.28. The LCNT transistors are connected through gate terminals to form the output node, OUT to which transistor $C_1$ is connected. In static mode (MODE= logic "1"), transistor $C_1$ is off and footer transistor $C_3$ is on. When (A,B) = (1,1), the node X is at logic "1" and the

output node is at logic “0”. Both the LCNTs are turned off in this case, which leads to increase in resistance of supply voltage to ground path. As a result, leakage current reduces. Similarly, for other inputs, analysis can be done in static mode.

In pre-charge phase of dynamic mode, transistor $C_1$ becomes on and pre-charges the output node to $V_{DD}$ as MODE=logic “0”, here the leakage is reduced as stacking effect is introduced due to LCNT transistors. In evaluation phase (MODE= logic “1”), transistor $C_1$ is off and $C_3$ is on. When (A,B) = (1,1), the output node is at logic “0”, due to which both the LCNTs are off and leakage current is reduced as stacking is introduced. Similar analysis can be done for other input combinations.

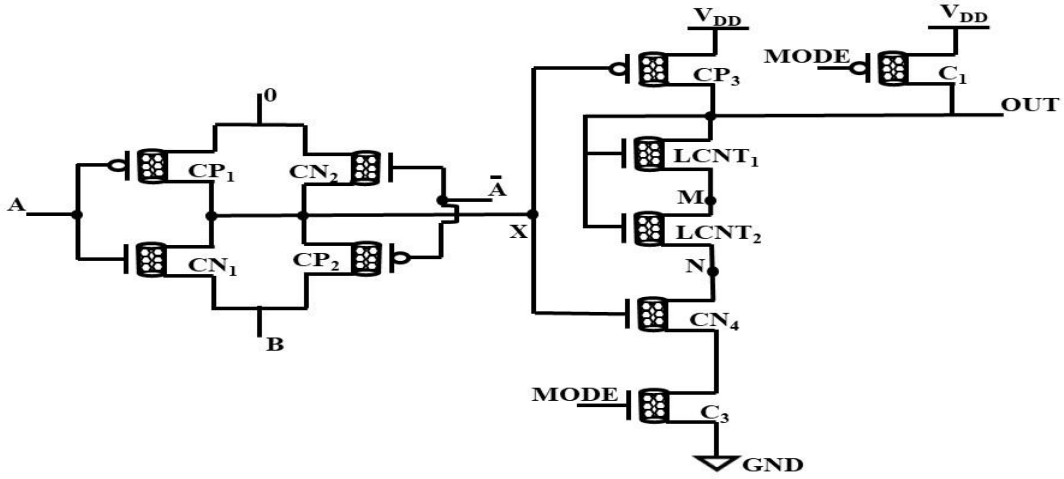



Fig. 5.28 Proposed LCNT based C-MDMTGDI 2-input NAND gate

### 5.5.2 Simulation results

This section is split into two segments. The first segment addresses functional verification of a 2-input NAND gate, while the second part involves a performance comparison of 2-input NAND gate, 2-input NOR gate, 2-input XOR gate, and 1-bit FA implemented using the proposed C-MDMTGDI based LECTOR, GALEOR and LCNT design with C-MDMTGDI design. The simulations are carried out using HSPICE tool with 32nm CNTFET Stanford model at 0.9V supply voltage and a load capacitance of 5fF. The proposed designs are designed using chiral indices of (17,0). However, for

C-MDMTGDI based GALEOR design, the GLTs are designed using chiral indices of (14,0) to ensure high threshold voltage for GLTs..

### 5.5.2.1 Functional verification

To illustrate the functionality of the proposed designs, the transient waveforms for 2-input NAND gate in static and dynamic mode are depicted in Fig. 5.29 and Fig. 5.30 respectively. For the comparison of the output voltage swing of the proposed designs with C-MDMTGDI and C-DMTGDI designs, the transient waveforms for C-MDMTGDI and C-DMTGDI are also displayed here. In static mode of all the designs, an output of logic "1" is generated by NAND gate if logic "0" is present in any of its inputs.

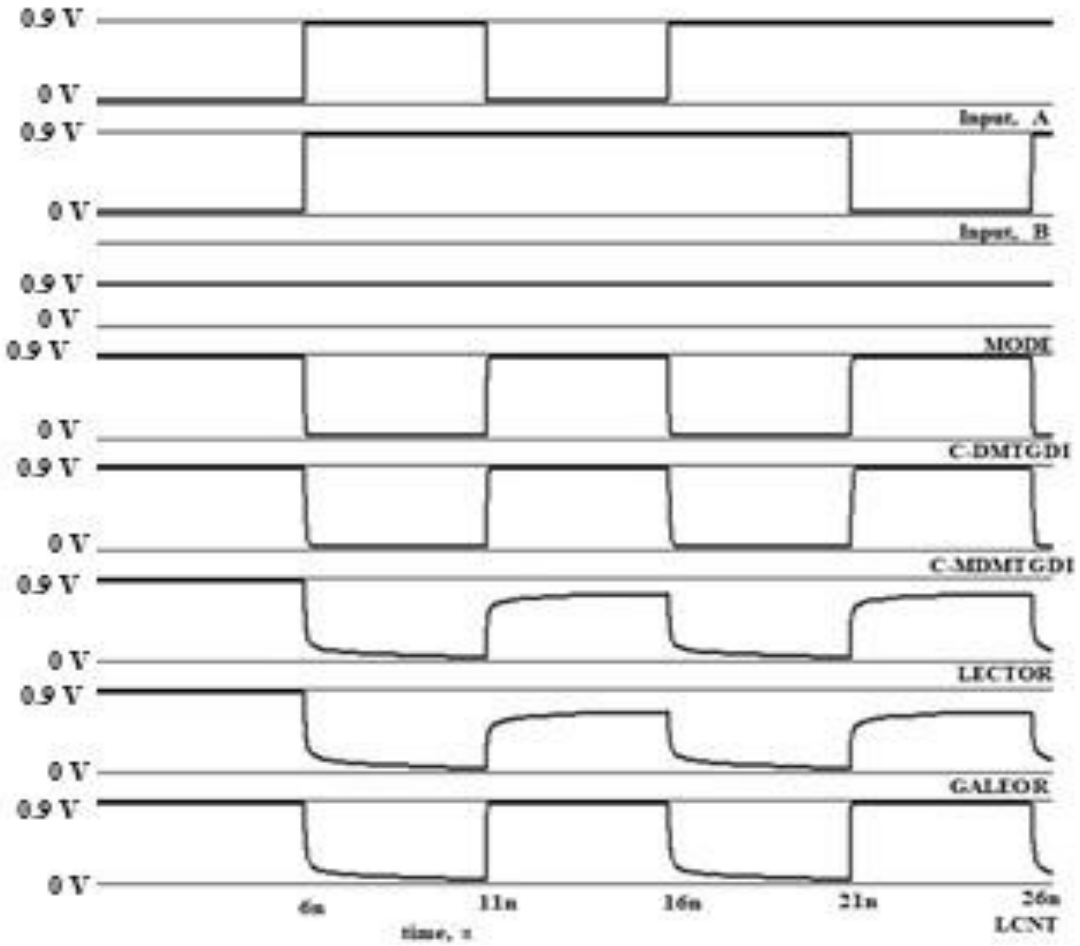



Fig. 5.29 Transient waveforms for LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI design of 2-input NAND gate at 32nm at 27℃ in static mode

In dynamic mode, as shown in Fig. 5.30, the MODE input is supplied with a clock signal having two phases of operation- pre-charge and evaluation. During the pre-charge phase, the MODE input is logic “0”, resulting in the charging of the output to the supply voltage for all designs. Conversely, in the evaluation phase, the MODE input is logic “1”. The NAND gate produces an output of logic “1” if any of its inputs are logic “0”, Therefore, the proposed designs based 2-input gate operate correctly in dynamic mode. However, the output voltage swing of the proposed C-MDMTGDI based LECTOR, GALEOR and LCNT designs is marginally degraded when compared to the C-MDMTGDI and C-DMTGDI designs.

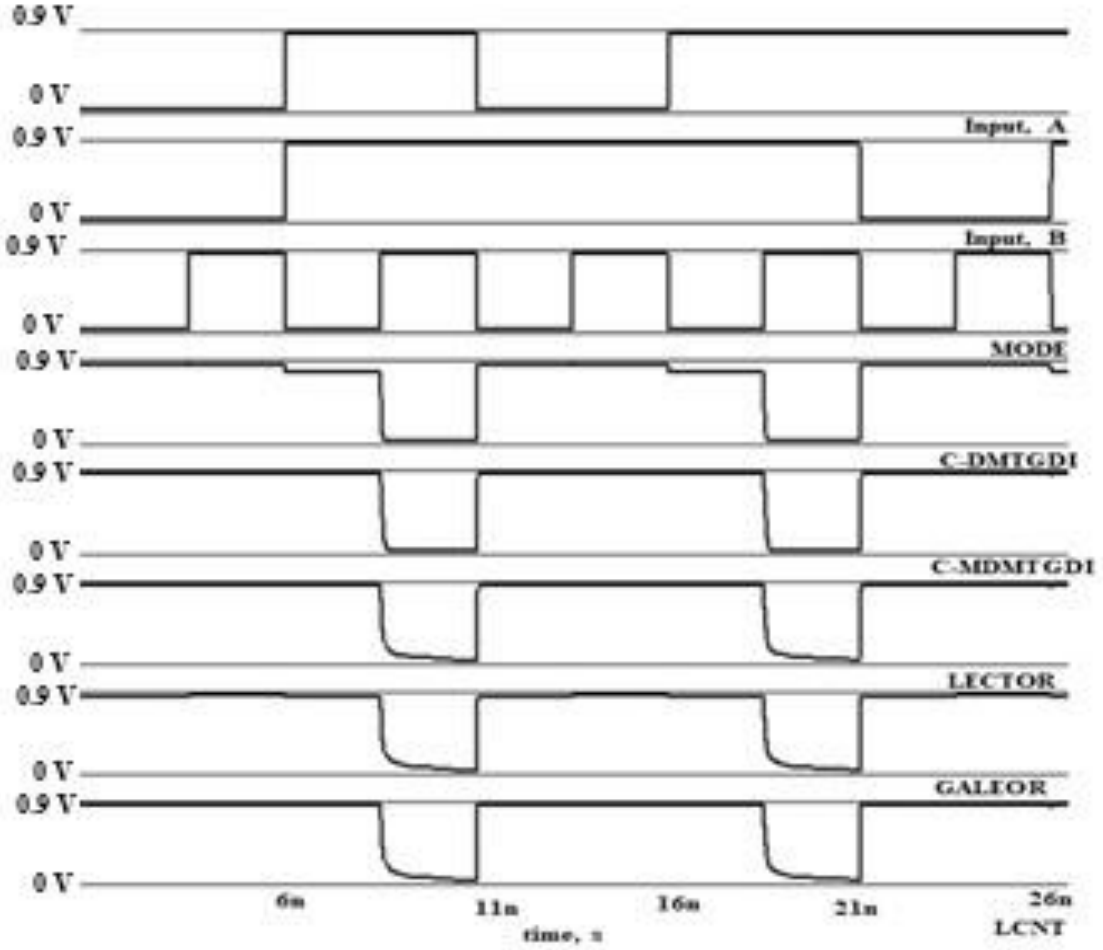



Fig. 5.30 Transient waveforms for LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI design of 2-input NAND gate at 32nm at 27℃ in dynamic mode

#### 5.5.2.2 Performance comparison

The proposed C-MDMTGDI based LECTOR, GALEOR and LCNT based 2-input NAND, NOR and XOR gates along with 1-bit FA circuit are simulated using 32nm CNTFET Stanford model in HSPICE tool at 0.9V and load capacitance of 5fF. The total leakage power is evaluated over all input combinations in both static and dynamic mode.

The total leakage power and delay values for 2-input NAND, NOR, XOR gates and 1-bit FA for C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI are enlisted in Table 5.3. Following are the observations from Table 5.3:

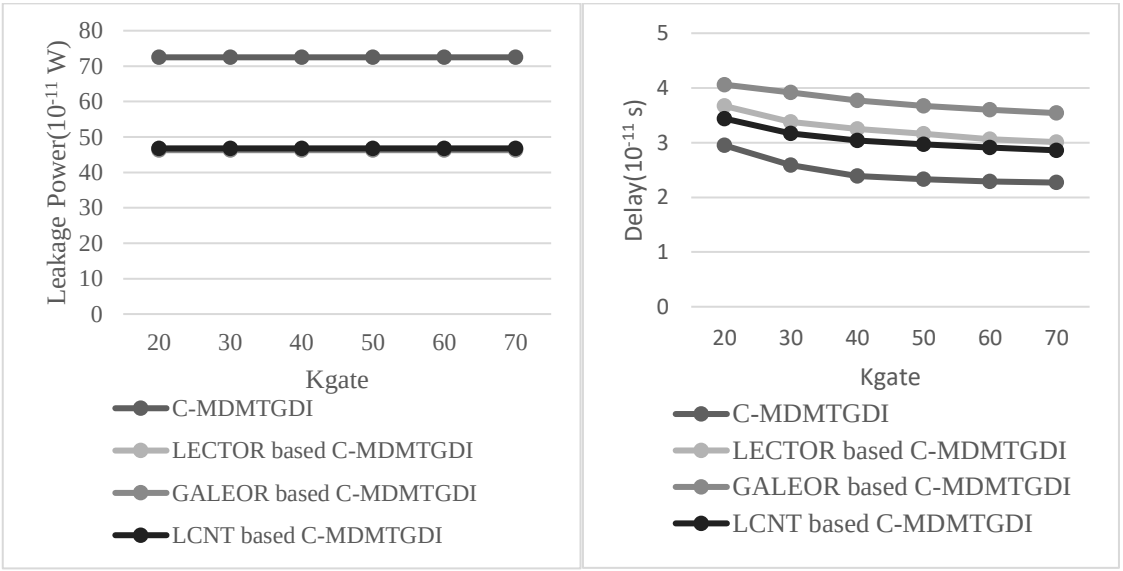
i. For 2-input gates, the proposed LECTOR based C-MDMTGDI offers a maximum leakage power reduction of 46.52% and 40.65% in static and dynamic mode respectively.
ii. For 1-bit FA circuit, the corresponding values are 35.47% and 28.83%.
iii. Similarly, for 2-input gates, the GALEOR-based C-MDMTGDI offers the most substantial leakage power reduction, with values reaching 46.68% and 40.94% in static and dynamic mode.
iv. In the case of a 1-bit FA circuit, these values are 36.18% and 29.54%.
v. Moreover, for 2-input gates, the LCNT based C-MDMTGDI design attains a maximum leakage power reduction of 46.5% and 40.75% in static and dynamic mode, respectively.
vi. For a 1-bit FA circuit, these reductions amount to 35.5% and 28.99%.
vii. The GALEOR based C-MDMTGDI design proves to be the most effective at reducing leakage power.

viii. Nevertheless, it is important to note that there is a trade-off, as each of these proposed leakage reduction techniques does result in a delay degradation.

Table 5.3 Leakage power and delay of C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND, NOR and XOR gates in static and dynamic mode at 32nm at 27°C

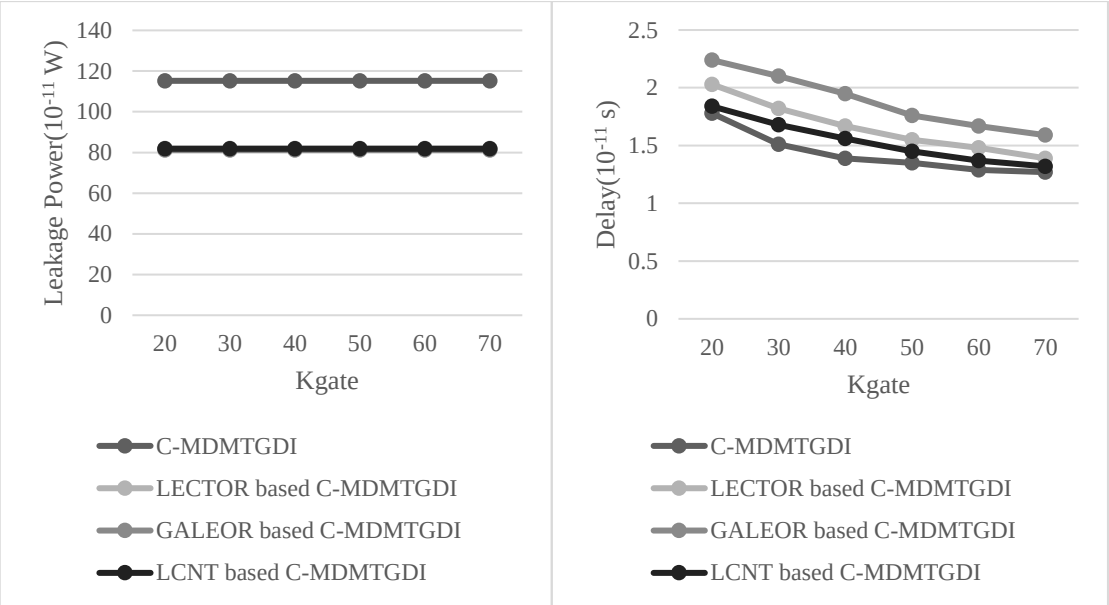
| Mode | Circuit | Leakage Power($10^{-11}$ W) | | | | Delay($10^{-11}$ s) | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | C-MDMTGDI | LECTOR based C-MDMTGDI | GALEOR based C-MDMTGDI | LCNT based C-MDMTGDI | C-MDMTGDI | LECTOR based C-MDMTGDI | GALEOR based C-MDMTGDI | LCNT based C-MDMTGDI |
| Static | | | | | | | | | |
| | NAND | 72.48 | 46.77 | 46.26 | 46.75 | 3.3 | 3.89 | 4.19 | 3.66 |
| | NOR | 114.56 | 61.27 | 61.08 | 61.29 | 3.26 | 3.99 | 4.04 | 3.9 |
| | XOR | 83.74 | 49.59 | 49.25 | 50.56 | 2.87 | 3.53 | 3.57 | 3.48 |
| | FA | 594.34 | 383.51 | 379.33 | 383.35 | 10.89 | 12.84 | 13.83 | 12.08 |
| Dynamic | | | | | | | | | |
| | NAND | 115.21 | 81.99 | 81.18 | 81.81 | 2.09 | 2.39 | 2.61 | 2.23 |
| | NOR | 191.95 | 113.92 | 113.36 | 113.73 | 1.99 | 2.33 | 2.46 | 2.17 |
| | XOR | 134.06 | 89.08 | 88.43 | 99.99 | 1.87 | 2.21 | 2.3 | 2.15 |
| | FA | 714.3 | 508.34 | 503.32 | 507.22 | 4.6 | 5.26 | 5.74 | 4.91 |

Additionally, an assessment was conducted to examine the impact of variations in oxide thickness ($T_{ox}$), dielectric constant ($K_{gate}$), and chiral indices on the leakage power and delay of the proposed designs, utilizing a 2-input NAND gate in both static and dynamic mode. In Fig. 5.31 and Fig. 5.32, the impact of changing the dielectric constant (Kgate) on leakage power and delay for C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND gate in static and dynamic mode is shown, respectively. It can be observed that the leakage power remains constant with variation in value of dielectric constant. However, the delay gets reduced as dielectric constant value increases due to lowered threshold voltage.




(a) (b)

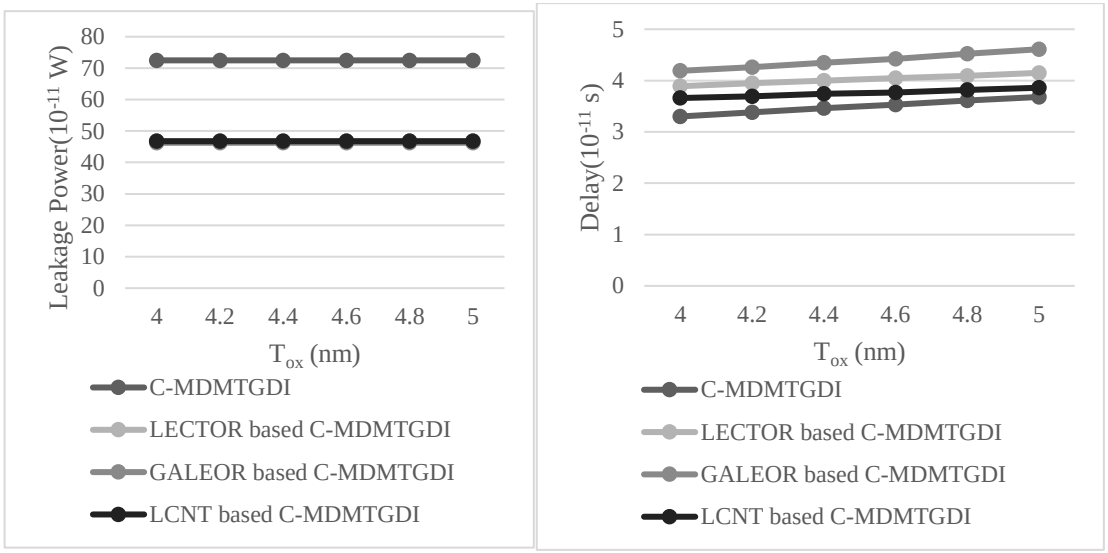
Fig. 5.31 Effect of variation of dielectric constant (Kgate) for C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND gate in static mode on (a) Leakage power (b) Delay




(a) (b)

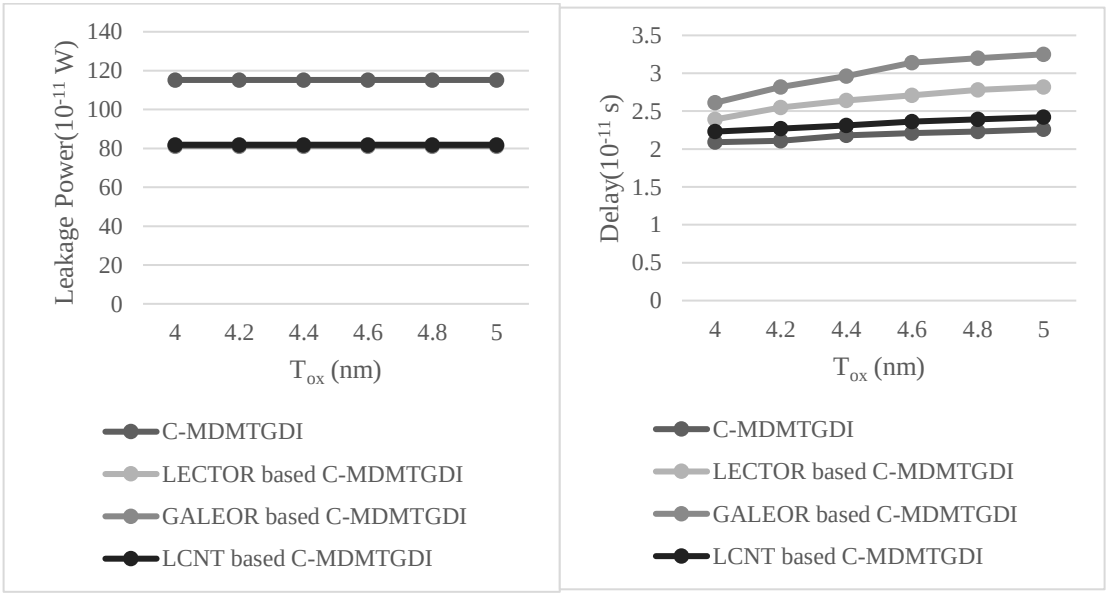
Fig. 5.32 Effect of variation of dielectric constant (Kgate) for C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND gate in dynamic mode on (a) Leakage power (b) Delay

Figure 5.33 and Figure 5.34 illustrate the effect of variations in oxide thickness ($T_{ox}$) on leakage power and delay for C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND gate in static and dynamic mode, respectively. It is evident that increase in oxide thickness ($T_{ox}$) has negligible impact on leakage power but the delay value is increased. This increase in delay is due to increase in threshold voltage in CNTFETs caused by the increased gate-channel capacitance resulting from the increased oxide thickness ($T_{ox}$).




(a) (b)

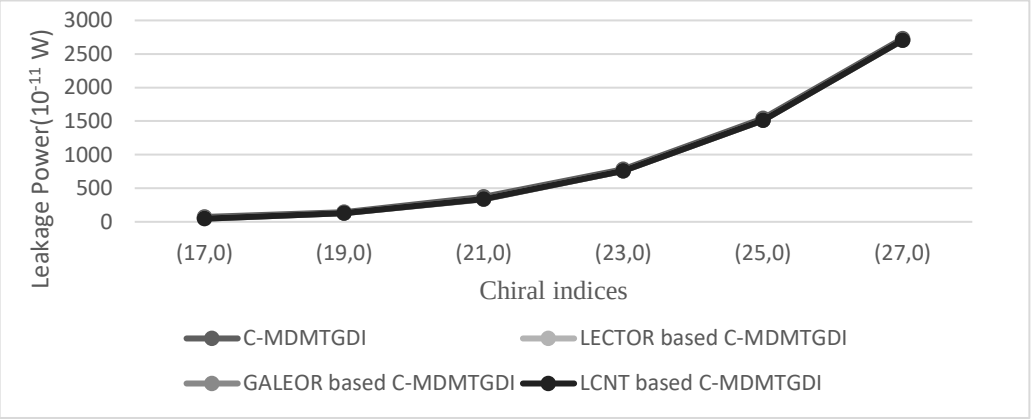
Fig. 5.33 Effect of variation of oxide thickness ($T_{OX}$) C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND gate in static mode on (a) Leakage power (b) Delay



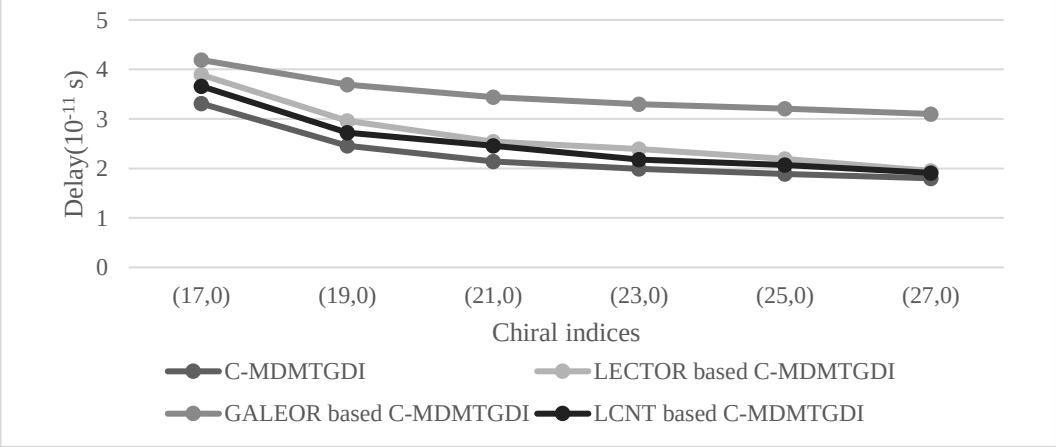

(a) (b)

Fig. 5.34 Effect of variation of oxide thickness ($T_{OX}$) C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND gate in dynamic mode on (a) Leakage power (b) Delay

The impact of varying chiral indices on leakage power and delay for C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND gate in static and dynamic mode is depicted in Fig. 5.35 and Fig. 5.36, respectively. It can be observed that the power of the proposed design increases while the delay value decreases. This is because as chiral indices' value increases, the diameter of CNTFETS increases, given by (5.2), as a result, the threshold voltage of CNTFETs decreases, given by (5.1).

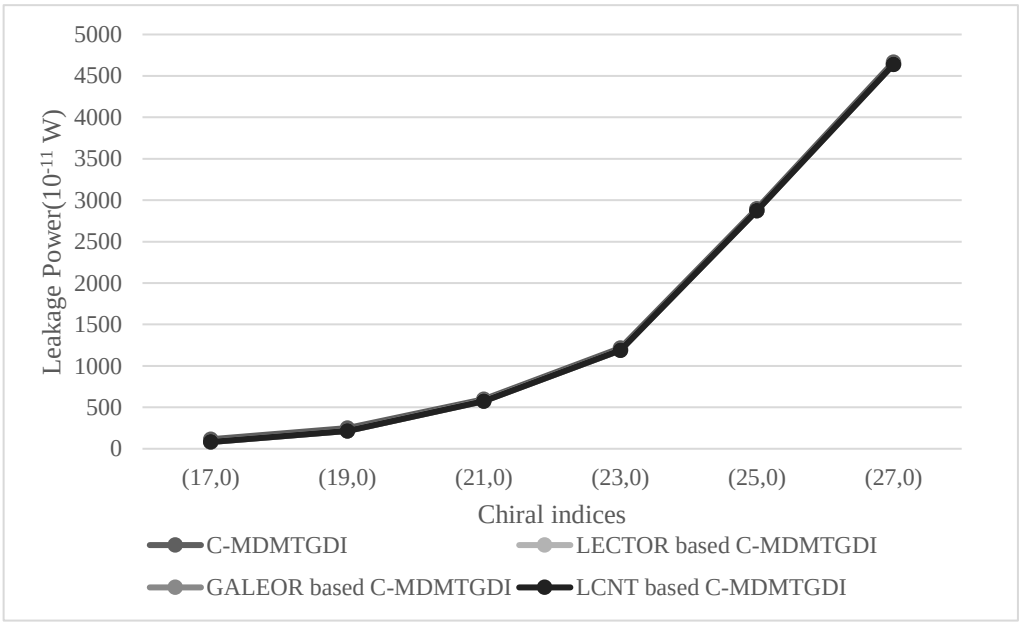



(a)

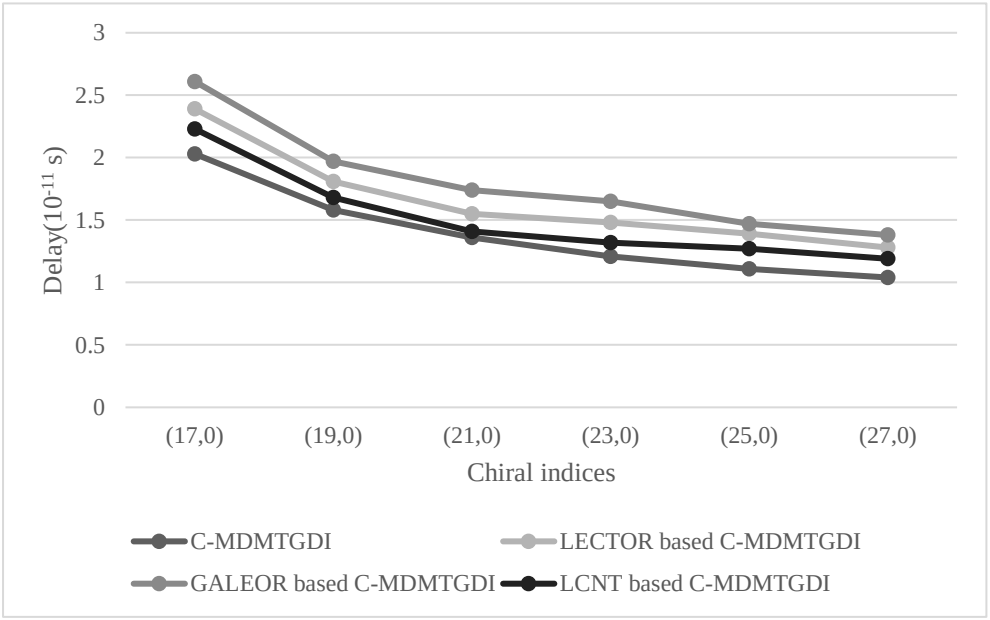



(b)

Fig. 5.35 Effect of variation of chiral indices for C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND gate in static mode on (a) Leakage power (b) Delay




(a)




(b)

Fig. 5.36 Effect of variation of chiral indices for C-MDMTGDI, LECTOR based C-MDMTGDI, GALEOR based C-MDMTGDI and LCNT based C-MDMTGDI for 2-input NAND gate in dynamic mode on (a) Leakage power (b) Delay

## 5.6 Conclusion

In this chapter, novel designs for footed DML and M-DMTGDI designs, based on CNTFETs, are introduced. These designs are referred to as C-DML and

C-MDMTGDI, respectively. The primary objective of these designs is to leverage the advantages of CNTFETs for its implementation. The proposed C-DML design allows the circuit to have both static and dynamic operating mode in a single structure. It provides benefits of CNTFETs to be incorporated in a footed DML design. The proposed C-MDMTGDI design overcomes the contention issue present in C-DMTGDI design. Further, leakage reduction techniques i.e., LECTOR, GALEOR and LCNT are implemented in the proposed C-MDMTGDI design. Extensive simulations are conducted to compare these designs in terms of power, delay, and PDP. The results of the simulations reveal that the proposed CNTFET based designs consistently outperform their CMOS counterparts, in terms of PDP reduction. In static mode, the proposed C-DML design achieves a maximum PDP reduction of 69.81% and 79.73% for 2-input gates type A and type B topologies, respectively and 60.61% for the 1-bit FA circuit compared to CMOS. In dynamic mode, the PDP reduction improves to 63.43% and 76.89% for 2-input gates, and 85.65% for the 1-bit FA. The proposed C-MDMTGDI design offers a maximum PDP reduction of 97.85% for 2-input gates in static mode and 93.82% in dynamic mode, with corresponding values of 87.71% and 89.21% for the 1-bit FA, as compared to CMOS counterparts. Compared to the C-DMTGDI design, the proposed C-MDMTGDI shows deteriorated PDP in static mode, but a significant improvement in dynamic mode. All simulation results are pre-layout, though post-layout results may vary by 10-15%.

Additionally, the performance of these designs under varying temperature, voltage and CNTFET parameters (dielectric constant, oxide thickness and chiral indices) is analysed. In proposed designs, increase in dielectric constant's value increase power but decrease delay, while an increase in oxide thickness raises threshold voltage, decreasing power and increasing delay. Additionally, increased chiral indices lower

threshold voltage, resulting in higher power but decreased delay. The proposed leakage reduction techniques prove to be efficient at reducing leakage power for C-MDMTGDI design. The proposed LECTOR-based C-MDMTGDI achieves a maximum leakage power reduction of 46.52% in static mode and 40.65% in dynamic mode for 2-input gates, with corresponding values of 35.47% and 28.83% for the 1-bit FA circuit. The GALEOR-based C-MDMTGDI provides similar reductions, with 46.68% and 40.94% for 2-input gates, and 36.18% and 29.54% for the 1-bit FA. The LCNT-based C-MDMTGDI achieves a leakage power reduction of 46.5% in static mode and 40.75% in dynamic mode for 2-input gates, with reductions of 35.5% and 28.99% for the 1-bit FA. The most efficient reduction of leakage power is achieved by the GALEOR based C-MDMTGDI design. However, it's worth noting that each of these proposed leakage reduction techniques results in a delay degradation. An increase in dielectric constant values show constant leakage power but reduced delay due to lowered threshold voltage. Oxide thickness insignificantly affects leakage power but increases delay due to increase in threshold voltage. An increase in chiral indices decrease the threshold voltage, resulting in increased power and decreased delay.

# Chapter 6

# Conclusion

This chapter summarizes the work done throughout the thesis and put forward the avenues of potential future work that could be built upon the base line principles established here.

## 6.1 Concluding Remarks

This thesis presents various alternative logic styles to implement designs which have low power, delay and PDP. Further, alternative logic styles based on improved transistor technology are also explored with special emphasis on having a design with low PDP. Various techniques are also used for leakage power reduction in MOSFET based and improved transistor technology based alternative logic styles. Chapter 2 presents an elaborative description of various alternative logic styles-DML, DCVSL and DMTGDI logic styles. For each alternative logic style, the operation and analysis of 2-input NAND gate is discussed.

In chapter 3, leakage reduction techniques (LECTOR and GALEOR), in context of static and dynamic CMOS, are incorporated in footed DML design. Proposed design-I incorporates LCTs with standard and high threshold voltage into footed DML design and the designs so arrived at, are called LDML and LDML-HIGH-VTH respectively. The proposed design-II employs GLT transistors with or without a footed diode transistor into footed DML design and resulting designs are referred to as GDML and GDMLD respectively. Extensive simulations are conducted to compare these designs in terms of leakage power, delay, and leakage PDP. The effect of temperature variation, voltage variation, technology scaling, and load capacitance variation is also delved into. Corner analysis is also done for all the proposed designs. The simulations show that LDML-HIGH-VTH is more efficient at leakage reduction than the LDML design, but it results in increased delay. Meanwhile, GDMLD saves more leakage power than GDML, but it also causes more delay. With technology scaling, the efficacy of the proposed designs

improves, although the leakage power increases, and the leakage power saving decreases with temperature rise. Increase in load capacitance causes an increase in delay, with GDMLD showing highest severity. The comparative analysis shows that while GDML and GDMLD are more efficient at leakage power saving, LDML has better leakage PDP due to lower delay.

Two novel designs, namely M-DMTGDI and DM-DCVSL, are proposed in chapter 4 and are referred to as proposed design-III and proposed design-IV, respectively. Proposed design-III addresses the contention issue in the existing DMTGDI design by embodying footed DML inverter in TGDI design. Proposed design-IV introduces dual mode functionality in existing static DCVSL design which allows static and dynamic mode of operation in a single structure. Extensive simulative investigation is done to analyse the proposed designs in terms of power, delay and PDP, while also checking the robustness of the proposed designs at different process corners. The effect of temperature and voltage variation is also investigated. The simulations show that both the proposed designs provide PDP reduction as compared to existing counterparts across all process corners. Comparative analysis show that the proposed design-III is adept at PDP reduction only when operated in dynamic mode for longer duration, however the proposed design-IV provides PDP reduction in both static and dynamic mode. Thus, proposed design-III exhibits higher performance for applications when the device is predominantly operated in dynamic mode of operation. As the supply voltage increases, the proposed designs exhibit an enhanced percentage reduction in PDP, yet it diminishes with a rise in temperature.

Chapter 5 presents two novel designs, namely C-DML and C-MDMTGDI design, which utilize CNTFETs, referred to as proposed design-V and proposed design-VI, respectively. These proposed designs aim to harness the advantages of CNTFETs for their

implementation. Extensive simulations have been carried out to comprehend these designs across a range of crucial parameters, such as power, delay, and PDP. Moreover, the performance of these designs has been evaluated under varying conditions of temperature, voltage and CNTFET parameters (dielectric constant, oxide thickness and chiral indices). The findings from these simulations consistently demonstrate superior performance of the proposed C-DML and C-MDMTGDI design over their CMOS counterparts, particularly in terms of reducing the PDP. Higher dielectric constants enhance power but reduce delay, while increased oxide thickness elevates threshold voltage, reducing power and increasing delay. Moreover, higher chiral indices decrease threshold voltage, which leads to increased power but reduced delay in proposed designs. Further, leakage reduction techniques-LECTOR, GALEOR and LCNT are also proposed for C-MDMTGDI design, referred to as proposed design-VII. Here, simulations are done to analyse the proposed designs in terms of leakage power, delay and leakage PDP. Additionally, an assessment was conducted to examine the impact of variations in oxide thickness, dielectric constant and chiral indices on the leakage power and delay of the proposed designs. Simulation results reveal that the GALEOR-based C-MDMTGDI design attains the maximum improvement in leakage power, followed by the LCNT-based C-MDMTGDI design and the LECTOR-based C-MDMTGDI design. It's worth noting that each of these proposed techniques for reducing leakage power results in a certain degree of delay degradation. An increase in dielectric constant values show constant leakage power but reduced delay due to lowered threshold voltage. Oxide thickness insignificantly affects leakage power but increases delay due to increase in threshold voltage. An increase in chiral indices decrease the threshold voltage, resulting in increased power and decreased delay.

## 6.2 Future Work

The emerging alternative logic styles and improved transistor technology offer great opportunity for low power designs with enhanced performance as compared to CMOS. By capitalizing on the unique features of alternative logic styles and improved transistor technologies, designers can overcome some of the limitations associated with conventional CMOS technology, thus paving the way for more efficient and capable electronic devices in the modern era.

Some of the avenues for future work that can be taken up are:

[1] As new applications emerge, such as IoT, wearable devices, and edge computing, the demands on circuits evolve. The proposed alternative logic styles, tailored to specific application requirements, can offer optimized solutions that CMOS might struggle to achieve.

[2] The future might witness hybrid designs that combine the strengths of alternative logic styles and CMOS technology. This design could harness the energy efficiency of alternative styles while leveraging CMOS for certain functions.

[3] Hybrid integration of improved transistor technology e.g., CNTFETs, with traditional MOSFET-based technologies can be done in the future. This design leverages the strengths of both materials for improved performance and functionality.

[4] The work on improved transistor technology can be further be explored to develop designs for satellite and space electronics due to their resilience to harsh environment and radiation.

# References


[1] G. K. Yeap, “Practical low power digital VLSI design”, Springer Science & Business Media, 2012.

[2] T. Sakurai, "Perspectives of low-power VLSI's," IEICE transactions on electronics, vol. 87, no. 4, pp. 429-436, 2004.

[3] A. Pal, “Low-Power VLSI circuits and systems” Springer, 2014.

[4] N. Weste and D. Harris, “CMOS VLSI Design: Pearson New International Edition: A Circuits and Systems Perspective”, 4th ed. London, England: Pearson Education, 2013.

[5] K. Bernstein et al., “High Speed CMOS Design Styles”, 1999th ed. Dordrecht, Netherlands: Springer, 2012.

[6] S.M. Kang, Y. Leblebici, and C. W. Kim, “CMOS Digital Integrated Circuits Analysis & Design”, 4th ed. New York, NY: McGraw-Hill Professional, 2014.

[7] I. Levi and A. Fish, “Dual Mode Logic: A New Paradigm for Digital IC Design”, 1st ed. Cham, Switzerland: Springer Nature, 2021.

[8] R. Zimmermann and W. Fichtner, “Low-power logic styles: CMOS versus pass-transistor logic,” IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, 1997.

[9] A. Morgenshtein, I. Shwartz, and A. Fish, “Gate Diffusion Input (GDI) logic in standard CMOS nanoscale process,” in 2010 IEEE 26-th Convention of Electrical and Electronics Engineers in Israel, 2010.

[10] A. Morgenshtein, A. Fish, and I. A. Wagner, "Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits," IEEE transactions on very large scale integration (VLSI) systems, vol. 10, no. 5, pp. 566-581, 2002.

[11] P. Bajpai, N. Pandey, K. Gupta, and J. Panda, "LECTOR incorporated differential cascode voltage swing logic (L-DCVSL)," Analog Integrated Circuits and Signal Processing, vol. 100, no. 1, pp. 221-234, 2019.

[12] P. Bajpai, N. Pandey, K. Gupta, S. Bagga, and J. Panda, "On improving the performance of dynamic DCVSL circuits," Journal of Electrical and Computer Engineering, vol. 2017, 2017.

[13] K. Gupta, V. Gosain, and N. Pandey, "Adiabatic Differential Cascode Voltage Switch Logic (A-DCVSL) for low power applications," J. King Saud Univ. - Eng. Sci., vol. 34, no. 3, pp. 180–188, 2022.

[14] I. Levi, A. Kaizerman, and A. Fish, "Low voltage dual mode logic: Model analysis and parameter extraction," Microelectronics journal, vol. 44, no. 6, pp. 553-560, 2013.

[15] A. Kaizerman, S. Fisher, and A. Fish, "Subthreshold Dual Mode Logic," IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 21, no. 5, pp. 979–983, 2013.

[16] I. Levi and A. Fish, "Dual mode logic—design for energy efficiency and high performance," IEEE Access, vol. 1, pp. 258–265, 2013.

[17] E. Rastegar Pashaki and M. Shalchian, "Design and simulation of an ultra-low power high performance CMOS logic: DMTGDI," Integration (Amst.), vol. 55, pp. 194–201, 2016.

[18] P. Sravani, H.P. Babu, Design of low power combinational adders using dual mode transmission gate diffusion input logic (DMTGDI), International Journal of Scientific Engineering and Technology Research, vol.6, pp. 3576-3580, 2017.

[19] I. Stanger, N. Shavit, R. Taco, L. Yavits, M. Lanuzza, and A. Fish, "Robust dual mode pass logic (DMPL) for energy efficiency and high performance," in 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020.

[20] S. A. Vitale, P. W. Wyatt, N. Checka, J. Kedzierski, and C. L. Keast, "FDSOI process technology for subthreshold-operation ultralow-power electronics," Proceedings of the IEEE, vol. 98, no. 2, pp. 333-342, 2010.

[21] A. Uchiyama, S. Baba, Y. Nagatomo, and J. Ida, "Fully depleted SOI technology for ultra-low power digital and RF applications," in 2006 IEEE international SOI Conferencee Proceedings, 2006: IEEE, pp. 15-16.

[22] J. Cai et al., "Will SOI have a life for the low-power market?" in 2008 IEEE International SOI Conference, 2008: IEEE, pp. 15-16.

[23] D. Bol, R. Ambroise, D. Flandre, and J.-D. Legat, "Sub-45nm fully-depleted SOI CMOS subthreshold logic for ultra-low-power applications," in 2008 IEEE International SOI Conference, 2008: IEEE, pp. 57-58.

[24] J.-P. Noel et al., "Multi-$V_T$ UTBB FDSOI device architectures for low-power CMOS circuit," IEEE Transactions on Electron Devices, vol. 58, no. 8, pp. 2473-2482, 2011.

[25] N. Planes et al., "28nm FDSOI technology platform for high-speed low-voltage digital applications," in 2012 Symposium on VLSI technology (VLSIT), 2012: IEEE, pp. 133-134.

[26] Q. Liu et al., "Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22nm node and beyond," in 2010 Symposium on VLSI Technology, 2010: IEEE, pp. 61-62.

[27] V. K. Magraiya and T. K. Gupta, "ONOFIC-based leakage reduction technique for FinFET domino circuits," International Journal of Circuit Theory and Applications, vol. 47, no. 2, pp. 217-237, 2019.

[28] S. Garg and T. K. Gupta, "SCDNDTDL: a technique for designing low-power domino circuits in FinFET technology," journal of computational electronics, 2020.

[29] X. Huang et al., "Sub 50-nm finfet: PMOS," in International Electron Devices Meeting 1999. Technical Digest (Cat. No. 99CH36318), 1999: IEEE, pp. 67-70.

[30] S. Garg and T. K. Gupta, "A 4: 1 multiplexer using low-power high-speed domino technique for large fan-in gates using FinFET," Circuit World, 2020.

[31] A. K. Dadoria, K. Khare, T. K. Gupta, and R. Singh, "Ultra-low power FinFET-based domino circuits," International Journal of Electronics, vol. 104, no. 6, pp. 952-967, 2017.

[32] A. K. Dadoria, K. Khare, T. K. Gupta, and R. Singh, "Ultra low power high speed domino logic circuit by using FiNFET technology," 2016.

[33] T. J. K. Liu, "FinFET history, fundamentals and future," in Proceedings of the Symposium on VLSI Technology Short Course, 2012: University of California.

[34] V. K. Magraiya and T. K. Gupta, "ONOFIC Pull-Up Approach in Domino Logic Circuits Using FinFET for Subthreshold Leakage Reduction," Circuits, Systems, and Signal Processing, vol. 38, no. 6, pp. 2564-2587, 2019.

[35] A. K. Dadoria, K. Khare, T. K. Gupta, and R. Singh, "New leakage reduction techniques for FinFET technology with its application," Journal of Circuits, Systems and Computers, vol. 27, no. 07, p. 1850112, 2018.

[36] W. Hoenlein et al., "Carbon nanotube applications in microelectronics," IEEE Transactions on components and packaging technologies, vol. 27, no. 4, pp. 629-634, 2004.

[37] A. T. Mahani and P. Keshavarzian, "A novel energy-efficient and high speed full adder using CNTFET," Microelectronics Journal, vol. 61, pp. 79-88, 2017.

[38] M. L. P. Tan, G. Lentaris, and G. A. Amaratunga, "Device and circuit-level performance of carbon nanotube field-effect transistor with benchmarking against a nano-MOSFET," Nanoscale research letters, vol. 7, no. 1, p. 467, 2012.

[39] P. A. G. Sankar and K. Udhayakumar, “MOSFET-like CNFET based logic gate library for low-power application: a comparative study,” J. Semicond., vol. 35, no. 7, p. 075001, 2014.

[40] P. K. Patel, M. Malik, and T. K. Gupta, "Low leakage CNTFETs based 9T SRAM cells using dual-chiral vector and multi-Vt technology," Journal of Nanoelectronics and Optoelectronics, vol. 13, no. 1, pp. 45-54, 2018.

[41] S. Garg and T. K. Gupta, "Low leakage domino logic circuit for wide fan-in gates using CNTFET," IET Circuits, Devices & Systems, vol. 13, no. 2, pp. 163-173, 2018.

[42] S. Lin, Y.-B. Kim, and F. Lombardi, "Design of a CNTFET-based SRAM cell by dual-chiral vector selection," IEEE Transactions on Nanotechnology, vol. 9, no. 1, pp. 30-37, 2009.

[43] S. K. Sinha, K. Kumar, and S. Chaudhury, "CNTFET: The emerging post-CMOS device," in 2013 International Conference On Signal Processing And Communication (ICSC), 2013: IEEE, pp. 372-374.

[44] V. Prasad and D. Das, "A Review on MOSFET-Like CNTFETs." Science & Technology Journal,2016, pp. 124-129.

[45] Y. Sun and V. Kursun, "Carbon nanotubes blowing new life into NP dynamic CMOS circuits," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 2, pp. 420-428, 2013.

[46] S. K. Sahoo, G. Akhilesh, R. Sahoo, and M. Muglikar, "High-performance ternary adder using CNTFET," IEEE Transactions on Nanotechnology, vol. 16, no. 3, pp. 368-374, 2017.

[47] J. Liang, L. Chen, J. Han, and F. Lombardi, "Design and evaluation of multiple valued logic gates using pseudo N-type carbon nanotube FETs," IEEE Transactions on Nanotechnology, vol. 13, no. 4, pp. 695-708, 2014.

[48] C. Goyal, J. S. Ubhi, and B. Raj, "A low leakage TG-CNTFET–based inexact full adder for low power image processing applications," International Journal of Circuit Theory and Applications, vol. 47, no. 9, pp. 1446-1458, 2019.

[49] N. Srinivasan, N. S. Prakash, D. Shalakha, D. Sivaranjani, and B. B. T. Sundari, "Power reduction by clock gating technique," Procedia Technology, vol. 21, pp. 631-635, 2015.

[50] D. K. Sharma, "Effects of different clock gating techinques on design," International Journal of Scientific & Engineering Research, vol. 3, no. 5, pp. 1-4, 2012.

[51] J. Shinde and S. Salankar, "Clock gating—A power optimizing technique for VLSI circuits," in 2011 annual IEEE India conference, 2011: IEEE, pp. 1-4.

[52] M. P. Dev, D. Baghel, B. Pandey, M. Pattanaik, and A. Shukla, "Clock gated low power sequential circuit design," in 2013 IEEE Conference on Information & Communication Technologies, 2013: IEEE, pp. 440-444.

[53] X. Wang and W. H. Robinson, "A low-power double edge-triggered flip-flop with transmission gates and clock gating," in 2010 53rd IEEE International Midwest Symposium on Circuits and Systems, 2010: IEEE, pp. 205-208.

[54] A. Strollo and D. De Caro, "Low power flip-flop with clock gating on master and slave latches," Electronics Letters, vol. 36, no. 4, pp. 294-295, 2000.

[55] A. S. Seyedi, S. H. Rasouli, A. Amirabadi, and A. Afzali-Kusha, “Clock gated static pulsed flip-flop (CGSPFF) in sub 100 nm technology,” in IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures (ISVLSI’06), 2006.

[56] V. Sundararajan and K. K. Parhi, "Synthesis of low power CMOS VLSI circuits using dual supply voltages," in Proceedings of the 36th annual ACM/IEEE Design Automation Conference, 1999, pp. 72-75.

[57] M. Allani and V. D. Agrawal, “Energy-efficient dual-voltage design using topological constraints,” J. Low Power Electron., vol. 9, no. 3, pp. 275–287, 2013.

[58] K. N. Jayaraman and V. Agrawal, “A four-transistor level converter for dual-voltage low-power design,” J. Low Power Electron., vol. 10, no. 4, pp. 617–628, 2014.

[59] S. Kesharwani, J. Taraporewalla, and D. Saha, “Single threshold TSO level converters for ultra-low power digital designs,” in 2022 IEEE 19th India Council International Conference (INDICON), 2022, pp. 1–6.

[60] Y. S. Dhillon, A. U. Diril, A. Chatterjee, and A. D. Singh, “Low-power dual V th pseudo dual V dd domino circuits,” in Proceedings of the 17th symposium on Integrated circuits and system design, 2004.

[61] P. Zhao et al., “Low-power clocked-pseudo-NMOS flip-flop for level conversion in dual supply systems,” IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 17, no. 9, pp. 1196–1202, 2009.

[62] S. A. Tawfik and V. Kursun, “Multi-Vth Level Conversion Circuits for Multi-VDD Systems,” in 2007 IEEE International Symposium on Circuits and Systems, 2007, pp. 1397–1400.

[63] M. S. Bhat, V. V. Rao, and B. V. Pai, "Implementation of dynamic voltage and frequency scaling for system level power reduction," in International Conference on Circuits, Communication, Control and Computing, 2014: IEEE, pp. 425-430.

[64] T. Kolpe, A. Zhai, and S. S. Sapatnekar, "Enabling improved power management in multicore processors through clustered DVFS," in 2011 Design, Automation & Test in Europe, 2011: IEEE, pp. 1-6.

[65] M. Elgebaly and M. Sachdev, "Variation-aware adaptive voltage scaling system," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 15, no. 5, pp. 560-571, 2007.

[66] B. Amrutur, N. Mehta, S. Dwivedi, and A. Gupte, “Adaptative techniques to reduce power in digital circuits,” J. Low Power Electron. Appl., vol. 1, no. 2, pp. 261–276, 2011.

[67] S. G. Narendra and A. P. Chandrakasan, “Leakage in nanometer CMOS technologies”, Springer Science & Business Media, 2006.

[68] J. Kao and A. Chandrakasan, "MTCMOS sequential circuits," in Proceedings of the 27th European Solid-State Circuits Conference, 2001: IEEE, pp. 317-320.

[69] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI," IEEE Transactions on Electron Devices, vol. 44, no. 3, pp. 414-422, 1997.

[70] A. J. Drake, N. Zamdmer, K. J. Nowka, and R. B. Brown, "Analysis of the impact of gate-body signal phase on DTMOS inverters in 0.13 um PD-SOI," in IEEE international SOI conference, 2003, pp. 99-100.

[71] T. Kuroda, T. Fujita, F. Hatori, and T. Sakurai, "Variable threshold-voltage CMOS technology," IEICE Transactions on Electronics, vol. 83, no. 11, pp. 1705-1715, 2000.

[72] Y.-T. Ho and T.-T. Hwang, "Low power design using dual threshold voltage," in ASP-DAC 2004: Asia and South Pacific Design Automation Conference 2004 (IEEE Cat. No. 04EX753), 2004: IEEE, pp. 205-208.

[73] P. Lakshmikanthan and A. Nunez, "VCLEARIT: a VLSI CMOS circuit leakage reduction technique for nanoscale technologies," ACM Sigarch computer architecture news, vol. 35, no. 5, pp. 10-16, 2007.

[74] Z. Chen, M. Johnson, L. Wei, and W. Roy, "Estimation of standby leakage power in CMOS circuit considering accurate modeling of transistor stacks," in Proceedings.

1998 International Symposium on Low Power Electronics and Design (IEEE Cat. No. 98TH8379), 1998: IEEE, pp. 239-244.

[75] J. C. Park, "Sleepy stack: A new approach to low power VLSI and memory," Georgia Institute of Technology, 2005.

[76] C. M. Reddy, S. Dhara, B. Srikanth, and P. Ramakrishna, “Designing a D-flipflop using novel sleep transistor technique,” in 2022 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), 2022.

[77] N. Hanchate and N. Ranganathan, "LECTOR: a technique for leakage reduction in CMOS circuits," IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 12, no. 2, pp. 196-205, 2004.

[78] T. K. Gupta and K. Khare, "Lector with footed-diode inverter: a technique for leakage reduction in domino circuits," Circuits, Systems, and Signal Processing, vol. 32, no. 6, pp. 2707-2722, 2013.

[79] T. Gupta, A. Pandey, and O. Meena, "Analysis and design of lector-based dual-Vt domino logic with reduced leakage current," Circuit World, 2017.

[80] S. Katrue and D. Kudithipudi, "GALEOR: Leakage reduction for CMOS circuits," in 2008 15th IEEE International Conference on Electronics, Circuits and Systems, 2008: IEEE, pp. 574-577.

[81] V. L. Rani, M. M. Latha, and A. S. Ramesh, "Galeorstack-a novel leakage reduction technique for low power VLSI design," International journal of computer applications, vol. 48, no. 8, 2012.

[82] R. Lorenzo and S. Chaudhury, "LCNT-an approach to minimize leakage power in CMOS integrated circuits," Microsystem Technologies, vol. 23, no. 9, pp. 4245-4253, 2017.

[83] M. Moradinezhad Maryan, M. Amini-Valashani, S. J. Azhari, “An input controlled leakage restrainer transistor-based technique for leakage and short-circuit power reduction of 1-bit hybrid full adders,” Int. J. Circuit Theory Appl. 2021, 49, 2382–2395.

[84] M. Moradinezhad Maryan, S. J. Azhari, and M. Amini-Valashani, “A self-control leakage-suppression block for low-power high-efficient static logic circuit design in 22 nm CMOS process,” Integration (Amst.), vol. 87, pp. 1–10, 2022.

[85] H. Mahmoodi-Meimand and K. Roy, "Diode-footed domino: A leakage-tolerant high fan-in dynamic circuit design style," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 3, pp. 495-503, 2004.

[86] S. Garg and T. K. Gupta, "Low power domino logic circuits in deep-submicron technology using CMOS," Engineering Science and Technology, an International Journal, vol. 21, no. 4, pp. 625-638, 2018.

[87] A. P. Shah, V. Neema, and S. Daulatabad, "DOIND: a technique for leakage reduction in nanoscale domino logic circuits," Journal of Semiconductors, vol. 37, no. 5, p. 055001, 2016.

[88] J. W. Chun and C. R. Chen, "A novel leakage power reduction technique for CMOS circuit design," in 2010 International SoC Design Conference, 2010: IEEE, pp. 119-122.

[89] K. Gavaskar, U. S. Ragupathy, and V. Malini, “Design of novel SRAM cell using hybrid VLSI techniques for low leakage and high speed in embedded memories,” Wirel. Pers. Commun., vol. 108, no. 4, pp. 2311–2339, 2019.

[90] H. Mohammadian, M. B. Tavakolib, F. Setoudeh, and A. Horri, “Introduction of a new technique for simultaneous reduction of the delay and leakage current in digital circuits,” Integration (Amst.), vol. 78, pp. 84–94, 2021.

[91] V. K. Sharma, M. Pattanaik, and B. Raj, "INDEP approach for leakage reduction in nanoscale CMOS circuits," International Journal of Electronics, vol. 102, no. 2, pp. 200-215, 2015.

[92] V. K. Sharma, M. Pattanaik, and B. Raj, "ONOFIC approach: low power high speed nanoscale VLSI circuits design," International Journal of Electronics, vol. 101, no. 1, pp. 61-73, 2014.

[93] B. C. Devnath and S. N. Biswas, "An Energy-Efficient Full-Adder Design Using Pass-Transistor Logic," 2019 2nd International Conference on Innovation in Engineering and Technology (ICIET), Dhaka, Bangladesh, 2019, pp. 1-6.

[94] S. Yuan, Y. Li, Y. Yuan, and Y. Liu, “Pass transistor with dual threshold voltage domino logic design using standby switch for reduced subthreshold leakage current,” Microelectronics, vol. 44, no. 12, pp. 1099–1106, 2013.

[95] M. Hasan, H. U. Zaman, M. Hossain, P. Biswas, and S. Islam, “Gate Diffusion Input technique based full swing and scalable 1-bit hybrid Full Adder for high performance applications,” Eng. Sci. Technol. Int. J., vol. 23, no. 6, pp. 1364–1373, 2020.

[96] N. Kandasamy, N. Telagam, and F. Ahmad, “A new approach for cyclic combinational circuit using TGDI,” Procedia Comput. Sci., vol. 143, pp. 645–652, 2018.

[97] S. Radhakrishnan, T. Nirmalraj, and R. K. Karn, “An enhanced Gate Diffusion Input technique for low power applications,” Microelectronics, vol. 93, pp. 104621, 2019.

[98] V. Yuzhaninov, I. Levi, and A. Fish, “Design flow and characterization methodology for dual mode logic,” IEEE Access, vol. 3, pp. 3089–3101, 2015.

[99] R. De Rose, P. Romero, and M. Lanuzza, “Double-precision Dual Mode Logic carry-save multiplier,” Integration (Amst.), vol. 64, pp. 71–77, 2019.

[100] S. Jacob, V. G. Menon, S. Joseph, and P. Sehdev, “Dual-mode power reduction technique for real-time image and video processing board,” J. Real Time Image Process., vol. 17, no. 6, pp. 1991–2004, 2020.

[101] K. Vicuña et al., “Energy efficient self-adaptive Dual Mode Logic address decoder,” Electronics (Basel), vol. 10, no. 9, p. 1052, 2021.

[102] A. Chauhan, K. K. Saini, N. Rajput, and R. Domah, “Implementation of High Performance 4-Bit ALU using Dual Mode Pass Transistor Logic,” in 2021 International Conference on Intelligent Technologies (CONIT), 2021.

[103] R. Escobar, L. M. Procel, L. Trojman, M. Lanuzza, and R. Taco, “High-speed and low-energy dual-mode logic based single-clack-cycle binary comparator,” in 2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS), 2021.

[104] R. Taco, L. Yavits, N. Shavit, I. Stanger, M. Lanuzza, and A. Fish, “Exploiting single-well design for energy-efficient ultra-wide voltage range dual mode logic-based digital circuits in 28nm FD-SOI technology,” in 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020.

[105] R. Taco, I. Levi, M. Lanuzza, and A. Fish, “Evaluation of Dual Mode Logic in 28nm FD-SOI technology,” in 2017 IEEE International Symposium on Circuits and Systems (ISCAS), 2017.

[106] A. K. Dadoria, K. Khare, T. K. Gupta, and N. Khare, “Integrating sleep and pass transistor logic for leakage power reduction in FinFET circuits,” J. Comput. Electron., vol. 16, no. 3, pp. 867–874, 2017.

[107] T. S. Kumar and S. L. Tripathi, “Leakage Reduction in 18 nm FinFET based 7T SRAM Cell using Self Controllable Voltage Level Technique,” Wirel. Pers. Commun., vol. 116, no. 3, pp. 1837–1847, 2021.

[108] Kajal and V. K. Sharma, “An efficient low power method for FinFET domino OR logic circuit,” Microprocess. Microsyst., vol. 95, no. 104719, pp. 104719, 2022.

[109] U. Mushtaq, M. W. Akram, D. Prasad, and B. C. Nagar, “A novel energy efficient and process immune Schmitt trigger circuit design using FinFET technology,” Indian J. Pure Appl. Phys., vol. 60, no. 5, pp. 387–394, 2022.

[110] U. Mushtaq, M. W. Akram, D. Prasad, and B. C. Nagar, “LCINDEP: a novel technique for leakage reduction in FinFET based circuits,” Semicond. Sci. Technol., vol. 38, no. 1, pp. 015003, 2023.

[111] H. M. N. Ahmad, M. S. Islam, K. M. Jameel, A. R. Ochi, and R. Hafiz, “Performance study of 12-CNTFET and GDI CNTFET based full adder in HSPICE,” in 2014 International Conference on Advances in Engineering & Technology Research (ICAETR - 2014), 2014.

[112] P. Tyagi, S. K. Singh, P. Dua, “14 transistors CNTFET and CMOS full adder cell for modified GDI technique,” International Journal of Innovative Technology and Exploring Engineering (IJITEE), vol. 8, no. 12, pp. 842–845, 2019.

[113] A. Sadeghi, R. Ghasemi, H. Ghasemian, and N. Shiri, “High efficient GDI-CNTFET-based approximate full adder for next-generation of computer architectures,” IEEE Embed. Syst. Lett., pp. 1–1, 2022

[114] M. Mohammadi, S. M. Zanjani, and M. Dolatshahi, “Design and simulation of a low PDP full adder by combining majority function and TGDI technique in CNTFET technology,” in 2022 12th International Conference on Computer and Knowledge Engineering (ICCKE), 2022.

[115] S. Maruthamuthu, “Ultra low power dual-gate 6T and 8T stack forced CNFET SRAM cells,” Microelectronics, vol. 44, no. 1, pp. 15–19, 2013.

[116] R. P. Somineni, B. K. Madhavi, and K. L. Kishore, “Low leakage CNTFET SRAM cells,” Procedia Comput. Sci., vol. 57, pp. 1049–1056, 2015.

[117] B. Pokharel, P. Gupta, and U. Dutta, “Designing CNTFET and Force Stacking CNTFET Inverter for the Analysis of Average Power and PDP at Different Low Supply Voltage”, International Journal of Engineering Research and Applications (IJERA) vol. 3, pp.1845-1855, 2013.

[118] R. P. Somineni, Y. P. Sai, and S. N. Leela, “Low leakage CNTFET full adders,” in 2015 Global Conference on Communication Technologies (GCCT), 2015.

[119] V. K. Magraiya, T. K. Gupta, and B. Garg, “Design of CNTFET based domino wide OR gates using dual chiral vector for reducing subthreshold leakage current,” Silicon, vol. 14, no. 14, pp. 8695–8706, 2022.

[120] S. Garg, T. K. Gupta, and A. K. Pandey, “A 4:1 Multiplexer using dual chiral vector CNTFET-based domino logic in nano-scale technology,” Int. J. Electron., vol. 107, no. 4, pp. 513–541, 2020.

[121] A. Kumar, B. P. Shrivastava, and A. Kumar, “A new leakage-tolerant domino circuit for wide fan-in gates with CNTFET,” in 2017 International Conference on Information, Communication, Instrumentation and Control (ICICIC), 2017.

[122] N. Mathur and S. Birla, “Performance evaluation and comparative analysis between traditional CNTFET based 9 T SRAM cells,” Silicon, vol. 14, no. 17, pp. 11749–11761, 2022.

[123] C.E. Jose, B. Kousalya, “Power reduction in CMOS sub-threshold dual mode logic circuits by power gating,” IOSR J. VLSI Signal Process, vol. 5, no. 2, pp. 60-67, 2015.

[124] P.V. Lakshmisree, M.C. Raghu, “Design of subthreshold DML logic gates with power gating techniques,” Int. J. Res. Eng. Technol., vol. 03, no. 04, pp. 174–180, 2014.

[125] P. Bikki and P. Karuppanan, "Low power and high performance multi-Vth dual mode logic design," 2016 11th International Conference on Industrial and Information Systems (ICIIS), Roorkee, India, 2016.

# Publications

**List of Journal Papers:**

[1] N. Yadav, N. Pandey, and D. Nand, **"Leakage reduction in dual mode logic through gated leakage transistors,"** Microprocess. Microsyst., vol. 84, no. 104269, pp. 1-12, 2021, doi: 10.1016/j.micpro.2021.104269. (SCI indexing, 3.503 IF)

[2] N. Yadav, N. Pandey, and D. Nand, **"Modified Dual Mode Transmission Gate Diffusion Input logic for improving energy efficiency,"** J. Circuits Syst. Comput., 2022, doi: 10.1142/S0218126623501712. (SCIE indexing, 1.5 IF)

[3] N. Yadav, N. Pandey, and D. Nand, **"LDML: A proposal to reduce leakage power in DML circuits,"** Wirel. Pers. Commun., vol. 129, no. 2, pp. 1009–1024, 2023, doi:10.1007/s11277-023-10170-4. (SCIE indexing, 2.2 IF)

**List of International Conference Papers:**

[1] N. Yadav, N. Pandey and D. Nand, **"CNTFET based Transmission Gate Diffusion Input Logic (C-TGDI) design,"** 2021 5th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT), Mysuru, India, 2021, pp. 701-705, doi: 10.1109/ICEECCOT52851.2021.9707944.

[2] N. Yadav, N. Pandey and D. Nand, "**LCNT incorporated domino with footed diode inverter**," 2021 8th International Conference on Signal Processing and

Integrated Networks (SPIN), Noida, India, 2021, pp. 839-843, doi: 10.1109/SPIN52536.2021.9566034.

[3] N. Yadav, N. Pandey and D. Nand, **"Energy Efficient CNTFET based Dual Mode Logic (C-DML) Design,"** 2023 Second International Conference on Electrical, Electronics, Information and Communication Technologies (ICEEICT), Trichirappalli, India, 2023, pp. 1-6, doi: 10.1109/ICEEICT56924.2023.10157144.

[4] N. Yadav, N. Pandey and D. Nand, **"Energy Efficient Dual Mode DCVSL (DM-DCVSL) design,"** 2023 Second International Conference on Electrical, Electronics, Information and Communication Technologies (ICEEICT), Trichirappalli, India, 2023, pp. 01-05, doi: 10.1109/ICEEICT56924.2023.10157481.

# Author's Biography

Neetika Yadav received her B.Tech in Electronics and Communication Engineering from Guru Gobind Singh Indraprastha University(GGSIPU), Delhi, India and M.Tech in VLSI Design from Guru Gobind Singh Indraprastha University(GGSIPU), Delhi, India. She is currently pursuing Ph.D. from Delhi Technological University (DTU), Delhi, India. Her area of research is low power VLSI.