M. Tech (Power Electronics and Systems)

Akib Azad

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COMPARISON OF DIFFERENT POWER FACTOR CORRECTION TOPOLOGIES

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SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
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IN
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I, **AKIB AZAD**, Roll No. 2K22/PES/01 student of M. Tech (Power Electronics & Systems), hereby declare that the project Dissertation titled **"COMPARISON OF DIFFERENT POWER FACTOR CORRECTION TOPOLOGIES"** which is submitted by me to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously submitted for the award of any Degree, Diploma.

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CERTIFICATE

I hereby certify that the project Dissertation titled **"COMPARISON OF DIFFERENT POWER FACTOR CORRECTION TOPOLOGIES"** which is submitted by Akib Azad, Roll No. 2K22/PES/01, Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diplomato this University or elsewhere.

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ABSTRACT

Power Factor Correction (PFC) is crucial for minimizing harmonic distortion and ensuring efficient power utilization in AC-DC converters. This thesis presents a comparative analysis of four popular PFC topologies: Boost PFC, Totem-Pole PFC, Totem-Pole PFC with MOSFET line rectification and Interleaved totem-pole PFC. Employing MATLAB Simulink, the performance is evaluated in terms of input power factor, THD, and efficiency.

This thesis offers valuable insights into the performance characteristics of diverse PFC topologies, aiding engineers and researchers in selecting the optimal solution for various applications with stringent power quality demands and efficiency considerations.

It also includes the performance analysis of 4kW on-board charger (OBC), designed to charge a lithium-ion battery used in an electric vehicle. It includes two stages of power conversion in which the first stage consists of an interleaved totem-pole based PFC converter, to convert the ac grid voltage into DC voltage without polluting the grid current and the second stage consists of a PSFB DC-DC converter to control the charging of the battery cells, while providing isolation between the grid and the battery

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LIST OF ABBREVIATIONS

THD	Total Harmonic Distortion
PFC	Power Factor Correction
FFT	Fast Fourier Transform
DBR	Diode Bridge Rectifier
EV	Electric Vehicle
p.f	Power Factor
SOC	State of Charge
EMI	Electro Magnetic Interference
PI	Proportional Integral
Ah	Ampere Hour
AC	Alternating Current
DC	Direct Current
PWM	Pulse Width Modulation
DCM	Discontinuous Conduction Mode
CCM	Critical Conduction Mode
SiC	Silicon Carbide
GaN	Gallium Nitride
PSFB	Phase Shifted Full Bridge

CHAPTER 1
INTRODUCTION

1.1 BACKGROUND

Power factor correction technology stands as a vital component within power electronic products, essential to fulfilling environmental standards. As diverse electrical devices draw electricity from the grid and international organizations enforce stricter requirements for grid regulations, power factor correction emerges as a focal point in advancing the power electronics sector. When the supply current from the source exhibits phase shift and significant harmonic distortion, it yields a diminished power factor, leading to energy wastage. This distorted current not only induces grid pollution but also causes a host of adverse effects. It results in voltage drops due to current flowing through line impedance, contributing to grid distortion [1]-[3].

Furthermore, it adversely impacts different circuits connected to the grid, leading to issues such as inaccuracies in instruments readings, malfunctioning of safety circuits, and rise in temperature of lines and distribution devices. Power factor correction technology stands as a vital component within power electronic products, essential to fulfilling environmental standards determined by the governments of numerous nations worldwide [4],[5].

The primary objective of integrating PFC into input supplies is to comply with global norms pertaining to p.f and harmonic content, ensuring alignment with regulatory requirements.

As power electronics technology leaps forward, driven by advancements in both Power Factor Correction (PFC) techniques and semiconductor development, optimizing converter efficiency has become a burning issue. The quest for better efficiency isn't just a technical pursuit; it has far-reaching implications for:

- Energy Conservation: Increased efficiency translates to less wasted energy, cutting back on our reliance on fossil fuels and greenhouse gas emissions.

- Reduced Operating Costs: Lower energy consumption translates to lower electricity bills for consumers and businesses alike.
- Enhanced Grid Stability: Efficient PFC minimizes harmonic distortion, making a cleaner, safe and more stable source to everyone connected to the grid.
- Smaller Footprints: Efficient designs require less bulky components, leading to compact and lightweight converters for space-constrained applications.

Generally, the traditional boost PFC circuit is extensively used for power PFC circuits, but its efficiency is reduced by 3-4% due to the diode bridge rectifier (DBR) [6]-[9]. To address this issue, new topologies have been developed to replace the DBR with devices having lower losses. One such topology is the bridgeless boost PFC , which replaces the DBR diodes with MOSFETs, resulting in lower conduction losses [10]-[12]. However, it may lead to a floating output relative to the input, causing high common mode electromagnetic interference (EMI). Another alternative is the totem-pole PFC, which also replaces the DBR diodes with MOSFETs arranged in a totem-pole configuration [13]-[15]. This topology incurs low conduction losses since only two semiconductor devices are active per half cycle of the AC source. Additionally, the load is not floating with respect to the input, resulting in better common mode EMI performance [3]. However, when using silicon MOSFETs in a totem pole arrangement, only DCM or CCM is possible [1]. In CCM, the reverse recovery of the MOSFET's body diode leads to heavy losses and reduced efficiency, which can be overcome by using SiC or GaN switches. Another topology, the Interleaved Boost PFC, offers improved supply quality and increase power density, mainly in Continuous Conduction Mode (CCM) operations. Although it requires more components, they are smaller in size, and experience reduced current strain per active component. Furthermore, it exhibits low EMI and better thermal performance compared to other topologies. However, because the control circuit requires two current sensors, its control is intricate and expensive in terms of hardware implementation [16]-[21].

1.2 LITERATURE REVIEW

Power factor must first be defined in order to fully understand Power Factor Correction (PFC). The ratio of real power to apparent power i.e cosø, is known as power factor. Apparent power is the overall power flowing between the source and the load, whereas real power is the energy used by the load. When all apparent power is transformed into real power, there are no reactive power losses, and the power factor will be at its ideal value of 1[2]

Power factor correction commonly uses switching power supplies. An AC waveform is usually converted into a DC waveform by a diode bridge in these supplies. The AC signal is rectified by the diode bridge, which has an impact on THD, and pf. Filters are occasionally employed to improve the power factor and smooth this rectified signal. These filters, have substantial power losses and require massive passive components due to which we use active topologies for the PFC[2]. MOSFET switching is used in active topologies, where the MOSFETs are controlled by a gate driver integrated circuit. Some of the active topologies discussed here are boost PFC, totem pole PFC, totem-pole PFC with MOSFET line rectification and Interleaved Totem-pole PFC.

1.2.1 Boost PFC

While there are several topologies available for implementing active PFC, the boost circuit architecture is still the very widespread choice in PFC applications because the filter inductor on the supply side of the boost topology produces a smooth, continuous waveform of supply current as opposite to the discontinuous waveform of supply current observed in buck or buck-boost configurations. An important benefit of this continuous input current is that filtering it is much simpler. Because of the capacitive loading of the line, further filtering on the converter input might raise costs and lower the p.f, improving the efficiency and economy of the boost circuit design. However, this topology has a disadvantage of limited power handling capabilities and low effficiency due to drop in the diode bridge rectifier. Fig. 1.1 displays the boost PFC circuit [2].

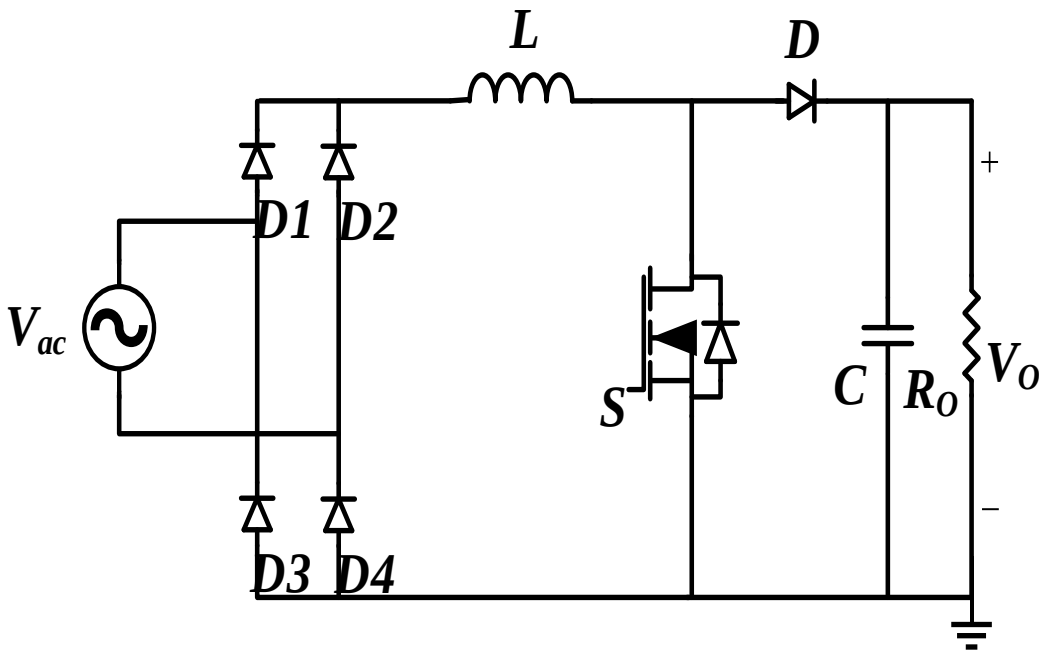


Fig. 1.1. Circuit diagram of Boost PFC

1.1.1 Totem-pole PFC

Totem-pole PFCs are a recent development in PFC topologies. With this active architecture, switches are employed in place of the diode rectifier bridge that is used in the conventional boost PFC. Due to that there is a decrease in the conduction losses and increase the overall efficiency. To control these switches and obtain unity power factor a complex control circuit is required for this topology. Fig. 1.2 displays the totem-pole PFC circuit[3].

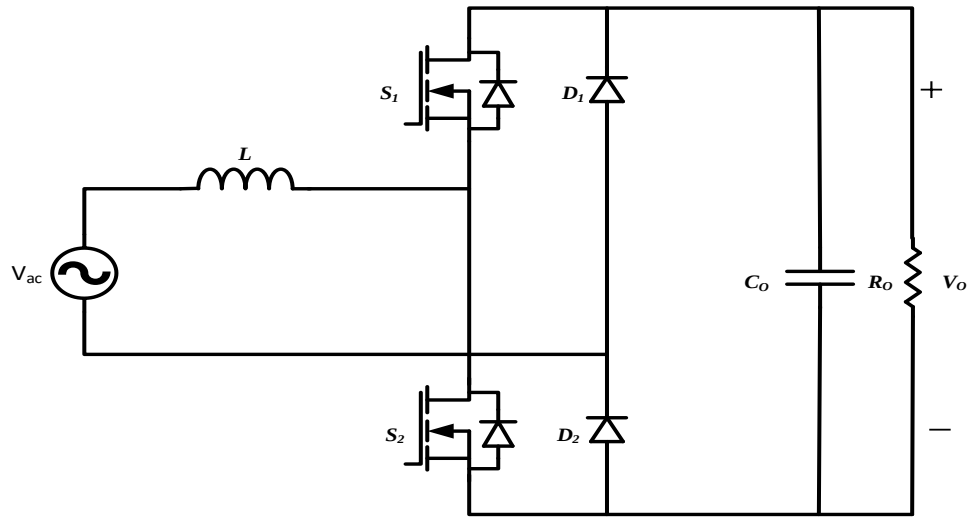


Fig. 1.2. Circuit diagram of Totem pole PFC

1.1.2 Totem-pole PFC with MOSFET line rectification

This configuration specifically changes the line rectifiers D_1 and D_2 in the Totem-Pole PFC with MOSFETs and are managed by two extra PWM circuits to synchronized with the supply cycle. This boosts the performance of the configuration further and reduces the conduction losses in the diode. Owing to the increased number of switches in these topologies, achieving unity power factor requires a sophisticated control circuit [3]. The figure of totem pole PFC with MOSFET line rectification is displayed in fig. 1.3.

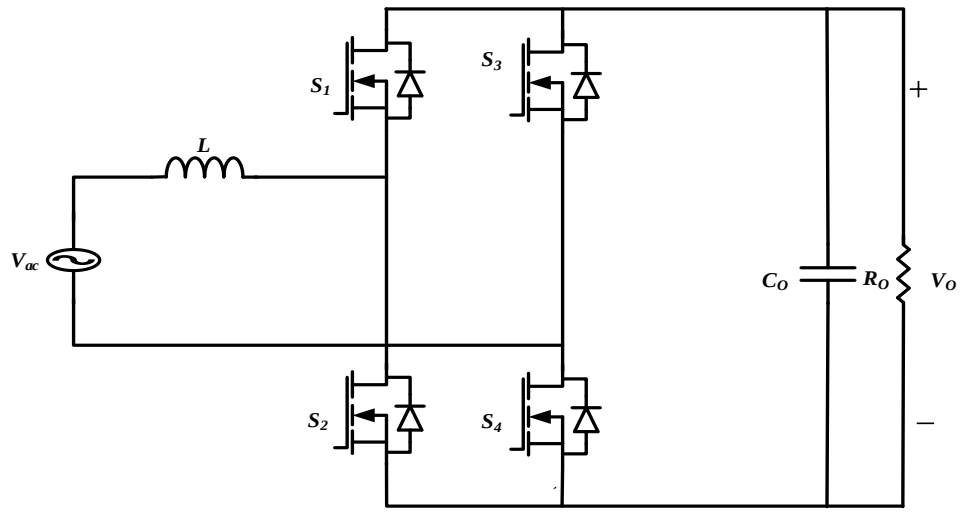


Fig. 1.3. Circuit diagram of Totem pole PFC with MOSFET line rectification

1.1.3 Interleaved Totem pole PFC

This configuration is an advanced topology designed to enhance power factor correction. By interleaving multiple phases, it effectively reduces the current ripple and improves overall efficiency. In this configuration, each phase operates with a totem-pole arrangement where the conventional line rectifiers are replaced by MOSFETs, controlled by synchronized PWM signals. This setup not only lowers conduction losses but also minimizes the electromagnetic interference (EMI), offering a robust solution for high-power applications. But this topology has a higher component count, higher cost and design complexity compared to other PFC topologies. Fig. 1.4 displays the Interleaved totem-pole PFC circuit[26].

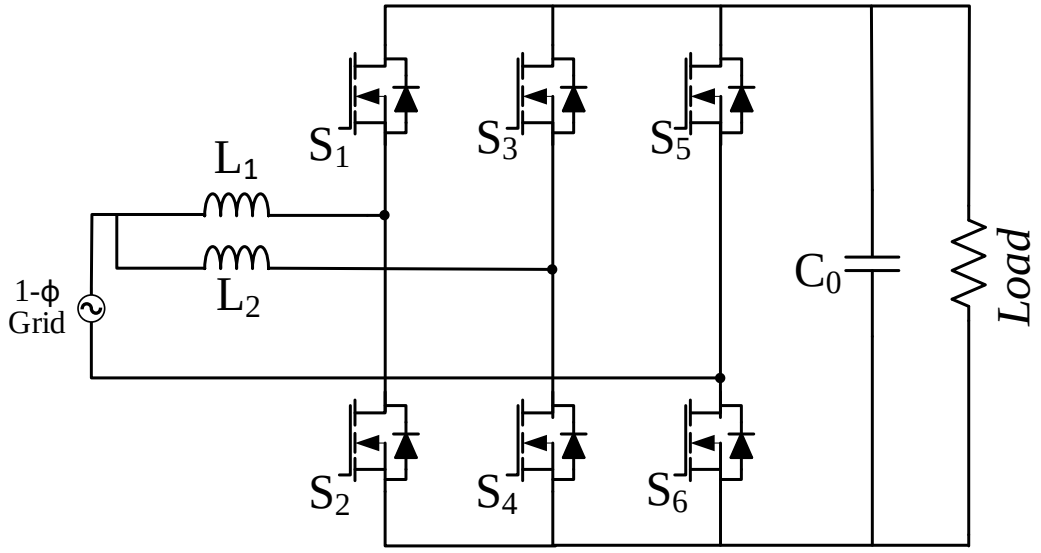


Fig. 1.4. Circuit diagram of Interleaved Totem pole PFC

1.3 THESIS MOTIVATION

The motivation behind this thesis arises from the urgent need to thoroughly evaluate and compare the performance metrics—namely input p.f, THD, and efficiency—of four significant PFC topologies: Boost PFC, Totempole PFC, Totempole PFC with MOSFET line rectification, and Interleaved Totempole PFC. These PFC

configurations represent major advancements in power electronics, each offering distinct advantages and operational efficiencies. This comparison aims to provide an in-depth understanding of their respective strengths and weaknesses with respect to key performance parameters. By analysing the input power factor, which indicates the effective utilization of power from the source, along with THD, which assesses the quality of the output waveform, and efficiency, which gauges the overall effectiveness of energy conversion, this study seeks to determine which topology excels in optimizing these critical aspects. This comparative analysis is intended to give numerous insights into the practical implementation and real-world analysis of these PFC topologies. The results of this study could assist engineers, researchers, and practitioners in choosing the most appropriate PFC topology based on specific application requirements, with the goal of enhancing power quality, efficiency, and reliability in various electrical systems and applications.

1.4 THESIS OBJECTIVE

The objective of this thesis is to thoroughly understand and compare the input p.f, THD, and efficiency of four distinct PFC topologies: Boost PFC, Totem-Pole PFC, Totempole PFC with MOSFET line rectification, and Interleaved Totempole PFC. This comparative investigation aims to provide a detailed knowledge of the performance characteristics of these topologies in terms of their input p.f, THD levels, and efficiency metrics. The specific objectives are:

1. Assess and compare the input p.f of Boost PFC, Totem-Pole PFC, Totempole PFC with MOSFET line rectification and Interleaved totempole PFC.
2. Compare the THD produced by each PFC topology.
3. Assess and compare the efficiency performance of Boost PFC, Totempole PFC, Totempole PFC with MOSFET line rectification, and Interleaved Totempole PFC to understand their energy conversion effectiveness and associated losses.

The results of this comparative study will shed light on the advantages and drawbacks of each PFC topology in relation to these key performance indicators.

This analysis is intended to assist engineers and researchers in choosing the most appropriate PFC topology for a particular application, with the aim of improving power quality and efficiency in diverse electrical systems.

1.5 THESIS ORGANIZATION

This thesis consists of complete design, control and analysis of the Boost PFC, Totempole PFC, Totempole PFC with mosfet line rectification and Interleaved totempole PFC. The outline of this thesis is shown below:

Chapter 1: This chapter gives a brief background of the research topic. It also provides motivation and objective of this thesis and then thesis organization.

Chapter 2: This chapter contain the analysis of Boost PFC converter which includes circuit diagram, modes of operation, closed loop control, design of parameters and simulation results. It also includes different gate driver circuits and current sensors

Chapter 3: This chapter comprise the investigation of Totempole PFC circuit which includes circuit diagram, modes of operation, closed loop control, design of parameters and simulation results.

Chapter 4: Here analysis of totem-pole PFC with mosfet line rectification is done which includes circuit diagram, modes of operation, closed loop control, design of parameters and simulation results.

Chapter 5: This chapter contains the investigation of Interleaved totempole PFC which includes circuit diagram, modes of operation, closed loop control, design of parameters and simulation results.

Chapter 6: It includes the design and analysis of a 4kw interleaved totempole PFC based on-board charger using PSFB dc-dc converter.

Chapter 7: The conclusion of the work is summarized, and future work is discussed.

CHAPTER 2
BOOST PFC CONVERTER

2.1 INTRODUCTION

Boost PFC is a circuit used to improve the p.f by using active electronic components, usually a boost converter.

DC-DC converters are essential in power electronics, bridging the gap between varying supply levels. Among them, the boost circuit is used for its ability to increase the output supply relative to its input, offering a versatile solution for power management. However, its application extends beyond voltage regulation. By incorporating power factor correction (PFC), boost converters can also contribute to maximizing efficiency and reducing harmonic distortion in AC power systems [6].

By improving the power factor, the system becomes more efficient. It reduces the reactive power and lowers the losses in power transmission. This can result in increased system capacity, and decreased stress on electrical components [8].

The boost converter's unique topology, featuring an inductor strategically placed on the input side, offers distinct advantages in terms of input current characteristics. Unlike buck or buck-boost converters, which exhibit discontinuous input currents, the boost converter fosters a continuous and inherently smoother input current waveform. This innate quality has far-reaching benefits for both cost-effectiveness and power quality.

2.2 CIRCUIT DIAGRAM

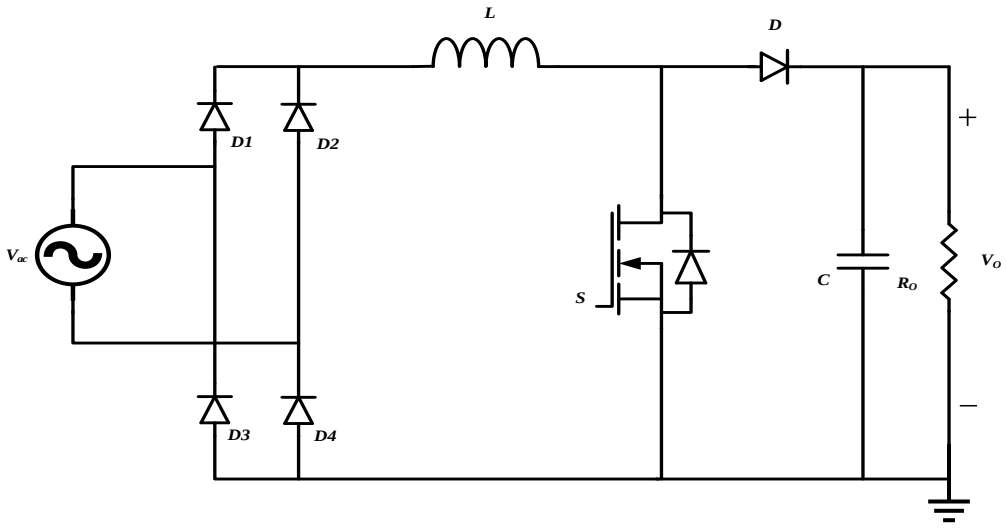


Fig. 2.1 Boost power factor correction converter

2.3 OPERATION MODE ANALYSIS

Positive Half Cycle Operation

While the mosfet *S* is on, the input supply charges the coil *L* through the diodes D_1, D_4 and load side capacitor provides the energy to the load.

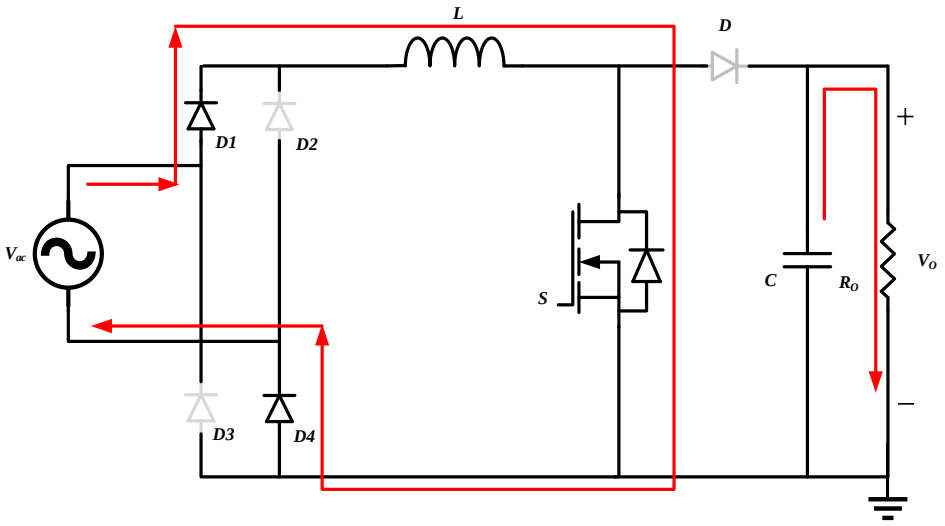


Fig. 2.2 Boost PFC when the switch is ON in positive cycle

When mosfet *S* is disabled, the coil *L* releases the power to the load by diodes D_1, *D* and D_4.

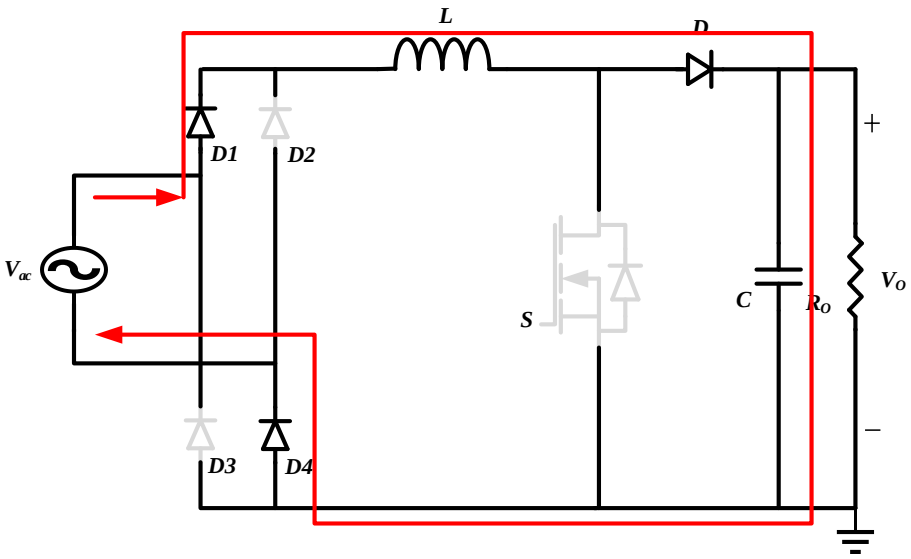


Fig. 2.3 Boost PFC while the switch is ON in negative cycle

Negative Half Cycle Operation

While the Mosfet *S* is enabled as displayed in Fig. 2.4, the input energies the coil *L* through the diodes D_2, D_3 and load capacitor provides the energy to the output.

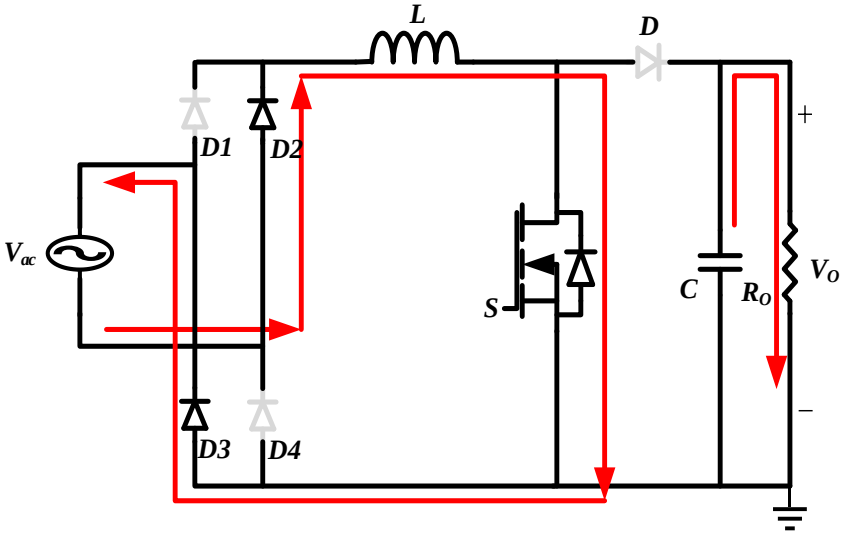


Fig. 2.4 Boost PFC while the switch is Off in negative cycle

When switch *S* is disabled, the coil *L* releases the power to the load by the diodes D_1, *D* and D_4.

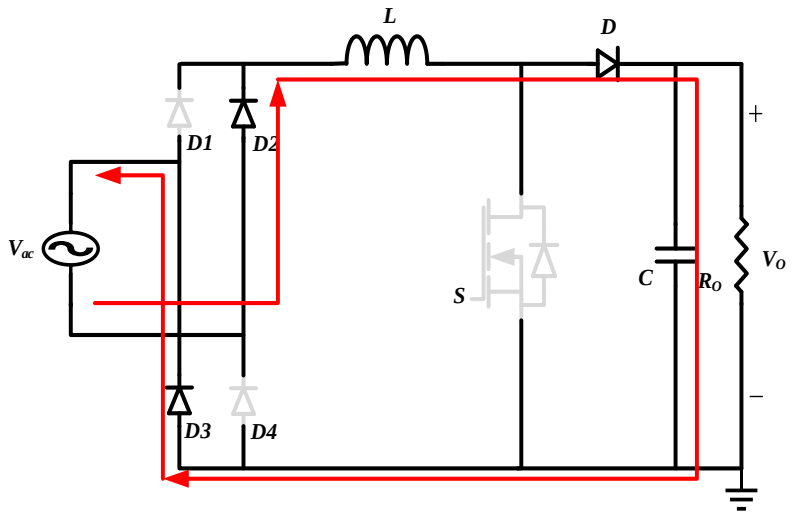


Fig. 2.5 Boost PFC Negative half cycle when switch is OFF.

2.4 CLOSED LOOP CONTROL OF BOOST PFC

The first phase begins by sensing the AC supply to create a sinusoidal reference signal used by the PI controller. Following this, a voltage regulator is utilized to manage the output voltage. Next in line is a current controller responsible for overseeing the inductor's current while upholding a sinusoidal waveform. Finally, the output is directed towards the PWM block, linked to trigger the MOSFET as displayed in Fig. 2.6.

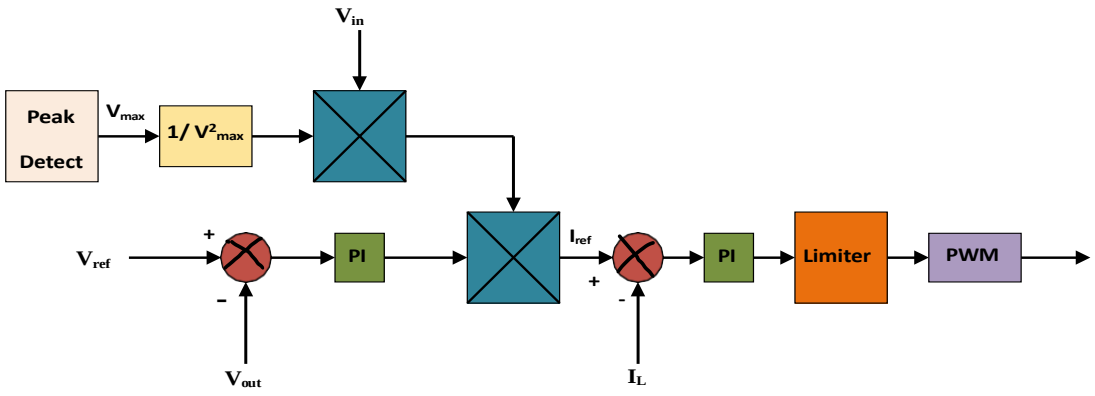


Fig. 2.6 closed-loop Boost PFC control

2.5 DESIGN OF BOOST PFC CONVERTER

Table 2.1. Design specifications for Boost converter

Supply (V_{in})	230 V
Load (V_o)	400 V
Power (P_o)	2500 W
Switching Frequency (f_{SW})	40kHz
Current Ripple (ΔI_L)	30%
Load Voltage Ripple (ΔV_c)	1% of output voltage
Load Resistance (R)	V_o^2/P_o
Inductor Resistance	60mΩ
ESR of Capacitor	40mΩ
Diode Forward Voltage drop	0.8 V
Inductor	330µH
Capacitor	4973µF

Additionally, to calculate the converters input inductor (L) and the output capacitor(C) we use the equations (2.1) and (2.2) respectively [3].

Inductor design

$$L = \frac{V_{in}^2}{\%Ripple * P_0 * f_{sw}} \left(1 - \frac{\sqrt{2} * V_{in}}{V_o}\right) \quad (2.1)$$

Capacitor Design

$$C_0 = \frac{P_0}{2\Pi * f_{line} * \Delta V_c * V_{bus}} \quad (2.2)$$

2.6 SIMULATION RESULTS

The boost PFC Circuit is simulated by MATLAB software, and the outcomes are depicted in Fig. 2.6 and Fig. 2.7, presenting the graphs of the supply voltage and supply current. As shown in fig. 2.8, the output remains steady at 400V. Additionally,

Fig. 2.9 showcases the characteristics of THD and fundamental current for the converter. For the proposed topology, an AC supply of 230V is used, and the inductor value was set at 0.330mH. The observation indicated synchronization between the load voltage and current of the circuit, signifying effective p.f correction. THD serves as a crucial performance metric, evaluating the quality of a power converter's output waveform. In this study, a simulation was conducted under specific operational parameters, including a supply voltage of 230V_{ac}, a switch mode frequency of 40 kHz, load resistance of 64Ω.

Input voltage waveform

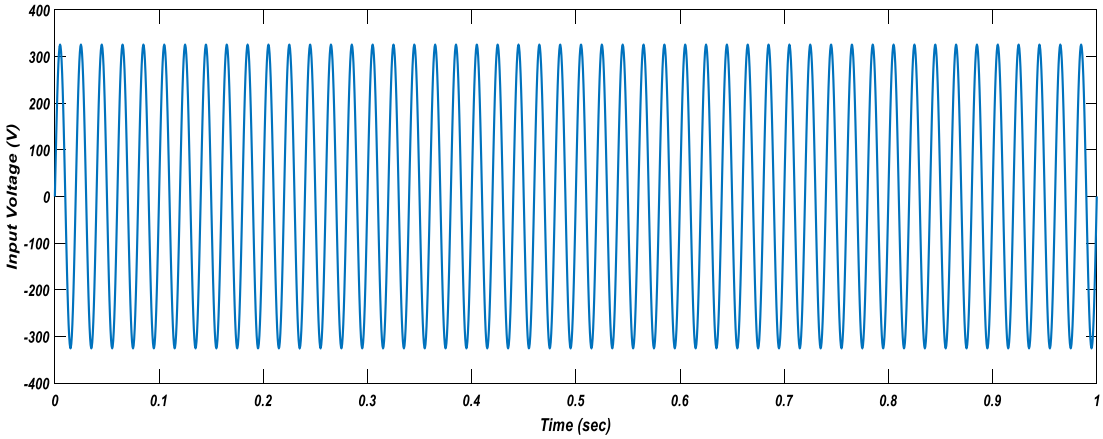


Fig. 2.7 Input voltage waveform of Boost PFC

Input current waveform

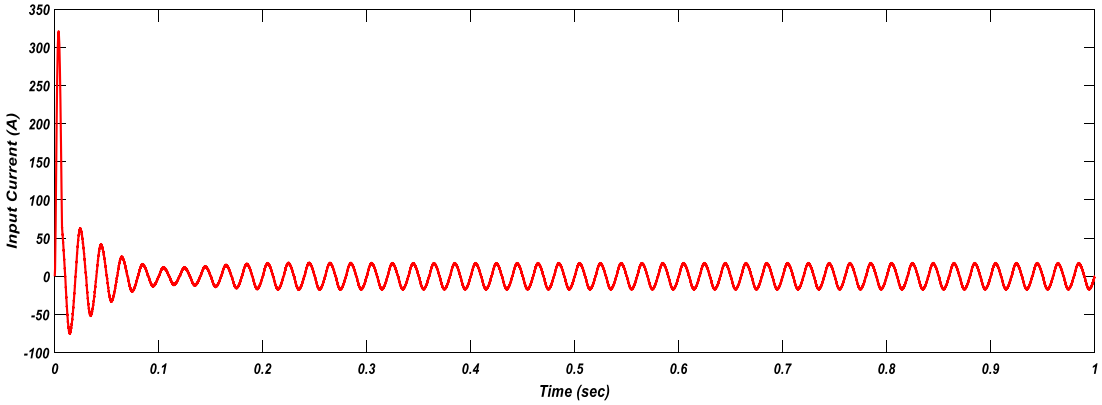


Fig. 2.8 Input current of Boost PFC

Output voltage waveform

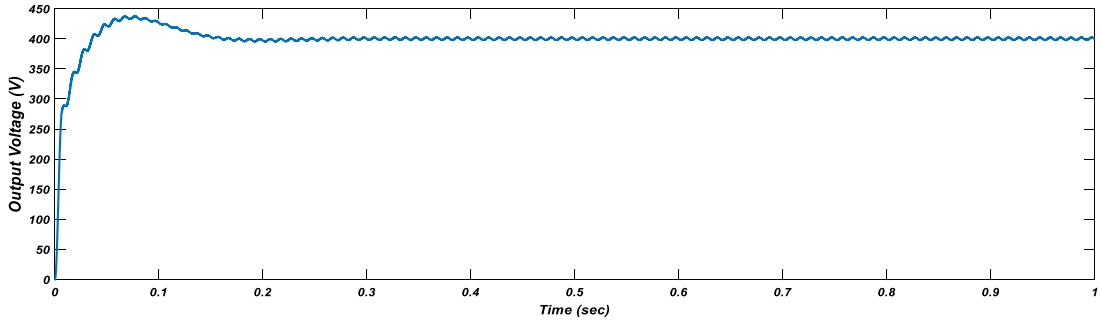


Fig. 2.9 Load voltage of Boost PFC

Output current

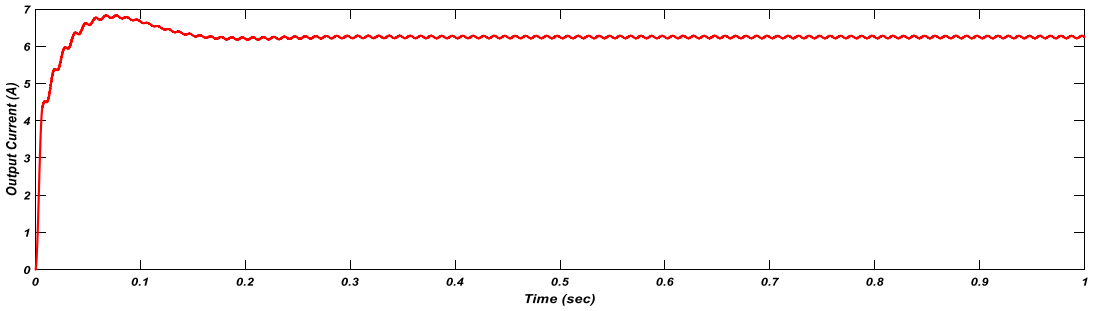


Fig. 2.10 Output voltage waveform of Boost PFC

FFT Analysis

THD is displayed in the below Fig. 2.11 which displays the Fundamental current is 16.41 Ampere and the THD is 4.48% in the input current i.e., harmonic is less than 5% of fundamental.

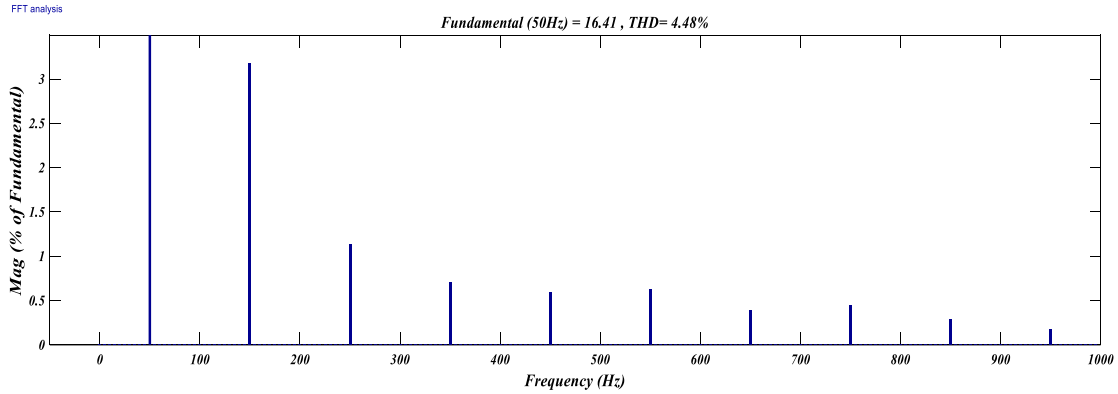


Fig. 2.11 FFT Analysis of Boost PFC

2.7 GATE DRIVER CIRCUIT

A gate driver IC functions as the intermediary link connecting the control signal, be it from digital or analog controllers to the power switches such as MOSFETs, IGBTs, SiC MOSFETs, among others.

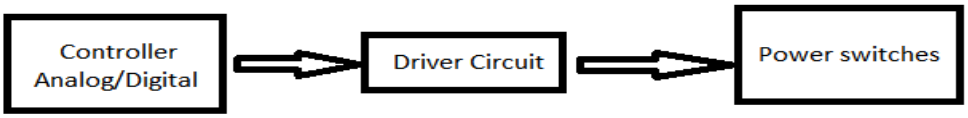


Fig. 2.13. Gate Driver Circuit

It typically comprises a level shifter combined with an amplifier.

Types of Gate Driver Circuit:

1) High-side driver circuit : They are specifically designed to control the power MOSFETs or IGBTs that operate with a positive power supply and are not grounded; they are essentially used for floating configurations [22].
   Example – Buck Converter.
2) Low-side driver circuit: It is used to trigger switches that are connected to negative supply of the source i.e. ground [23].
   Example – Boost converter.
3) Dual gate drivers: They are used to drive switches that have both low-side and high-side circuits.
   Example: Half – bridge converter.

Requirements of the driver circuit to be satisfied:

1) It should supply the required voltage and current to the gate source region.

2) It should provide isolation.

3) It should be able to work with floating supply.

4) It should be able to do the level shifting.

5) It should have high input impedance so that it does not absorb much current and load the controller.

2.7.1 High side gate driver circuit of buck converter:

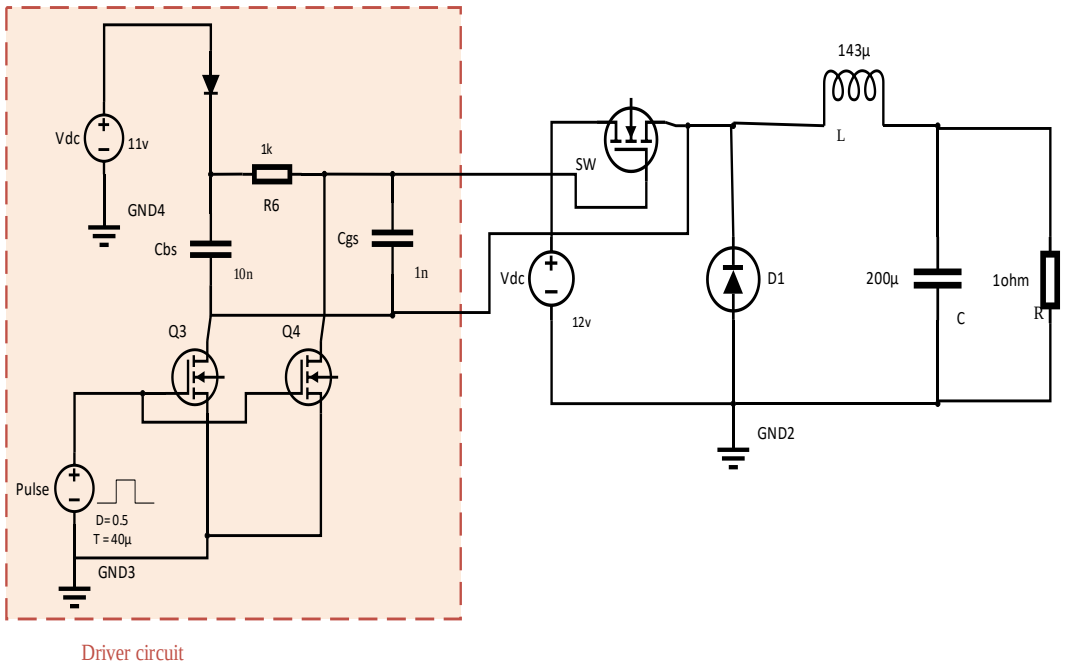


Fig. 2.14. Bootstrap based gate driver circuit for Buck Converter

In this gate driver circuit when the pulse from the controller is high then the NMOS Q3 and Q4 are on and the bootstrap capacitor get charged from the Vdc supply. When the pulse is low, then the NMOS Q3 and Q4 are turned off and the stored energy of the capacitor is used to trigger the buck circuit switch.

Table 2.2. Design Parameters of gate driver for Buck converter

Buck Converter	**Driver Circuit**
Input voltage = 12V	Microcontroller pulse of 5V
Inductor = 143µH	Duty Ratio = 0.5
Capacitor = 200µF	Rise time = 1ns
Resistance = 1Ω	Fall time = 1ns
Duty cycle = 50%	Time period = 40ns
Switching Freq = 25khz.	Bootstrap capacitor = 10nf.

2.7.2 Simulation Results

Microcontroller Output waveform

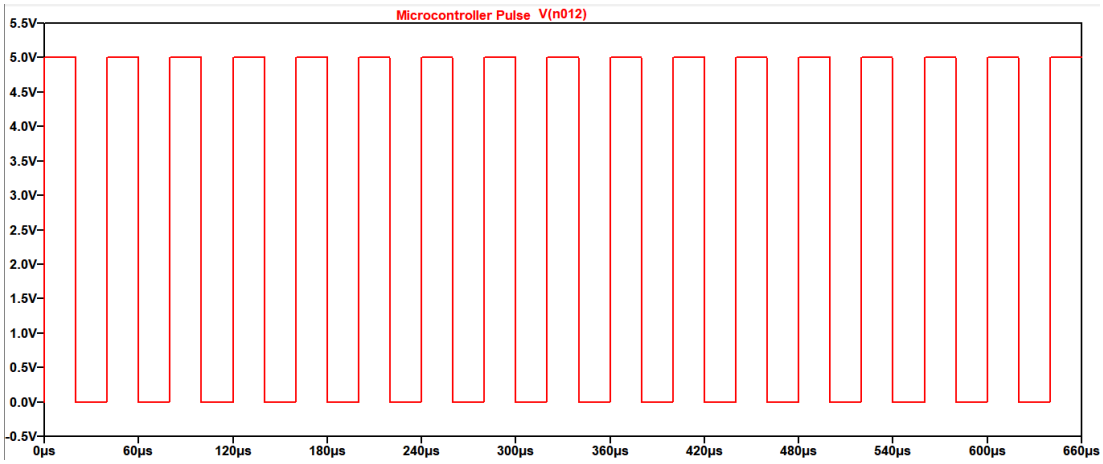


Fig. 2.15. Microcontroller output waveform

Driver Circuit output waveform

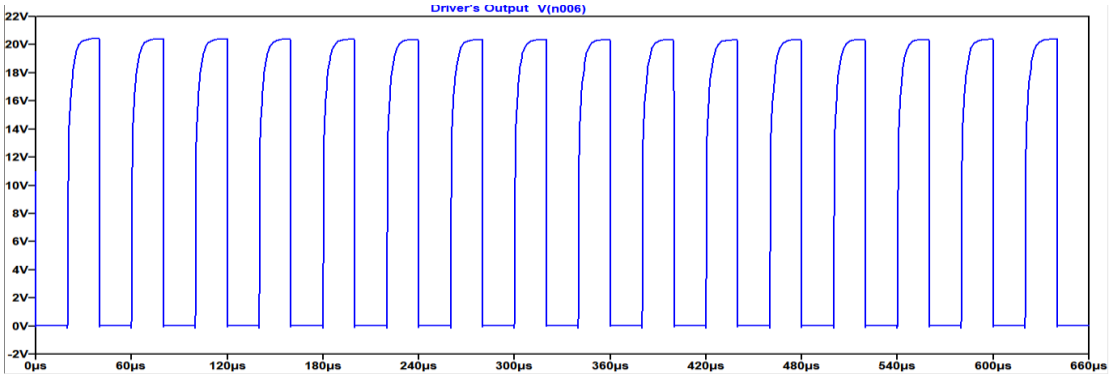


Fig. 2.16. High side Driver circuit output waveform

Advantage:

Bootstrapping method of gate driver is an inexpensive method to obtain floating supply.

Disadvantage:

We must charge and discharge the bootstrap capacitor at every switching cycle because of which the duty cycle and ON time of the converter gets limited.

2.7.3 Low side gate driver circuit of Boost converter:

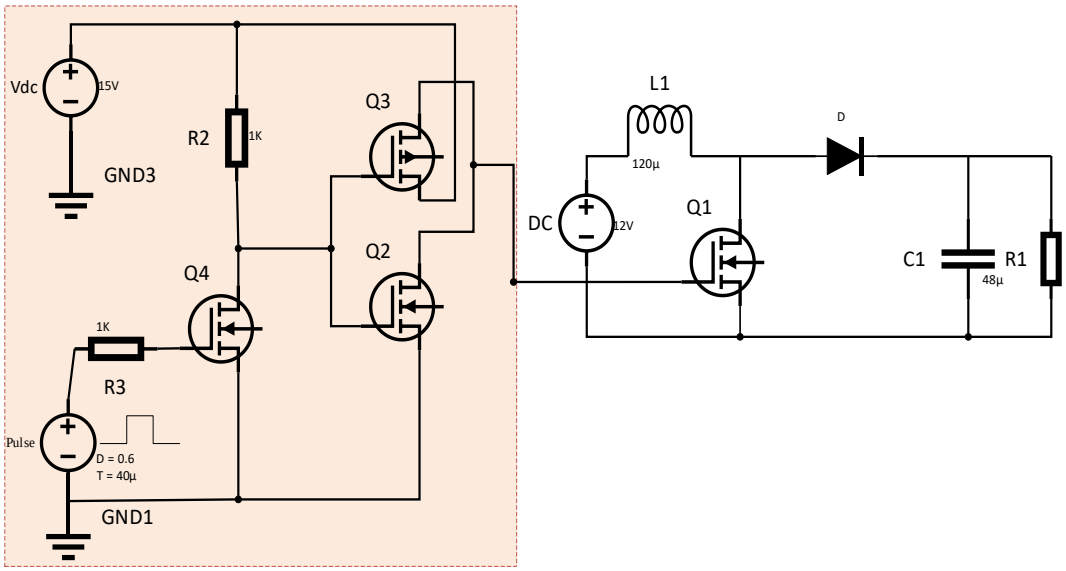


Fig. 2.17. Totem-pole based gated driver circuit for boost converter

In this boost driver circuit when the pulse from the controller is high, it switches on the NMOS Q4 and as a result ground voltage is applied to PMOS Q3 which make it on and supply voltage is delivered to the boost low side switch. When the pulse is low then the supply voltage is applied to the NMOS Q2 which results in ground voltage pass to the boost switch.

Table 2.3. Design Parameters for gate driver circuit of Boost converter

Boost Converter	**Driver Circuit**
Input voltage = 12V	Microcontroller pulse of 3.3V
Inductor = 120µH	Duty Ratio = .6
Capacitor = 48µF	Rise time = 1ns
Resistance = 50Ω	Fall time = 1ns
Duty cycle = 60%	Time period = 40ns
Switching Freq = 25khz.	External source = 15v

2.7.4 Simulation Results

Microcontroller output waveform

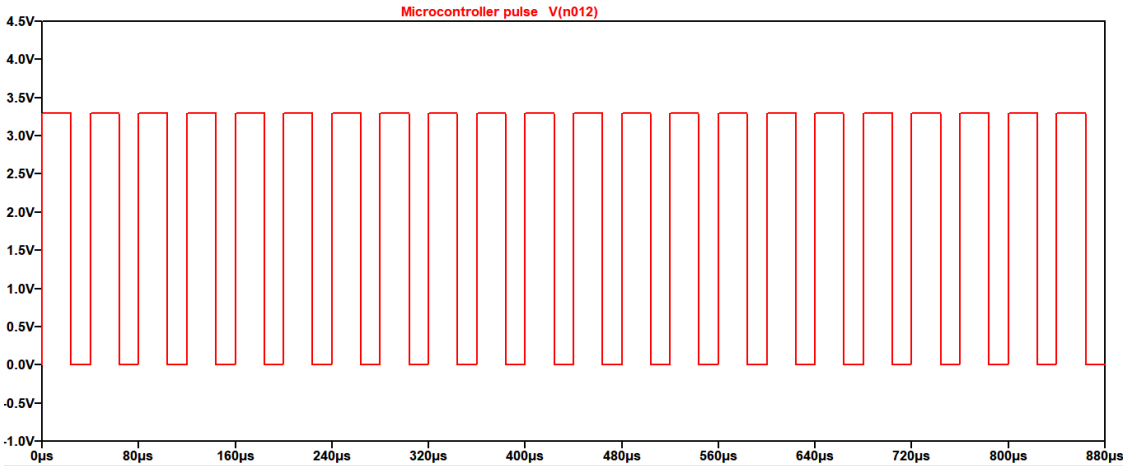


Fig. 2.18. Microcontroller output waveform

Driver circuit output Waveform

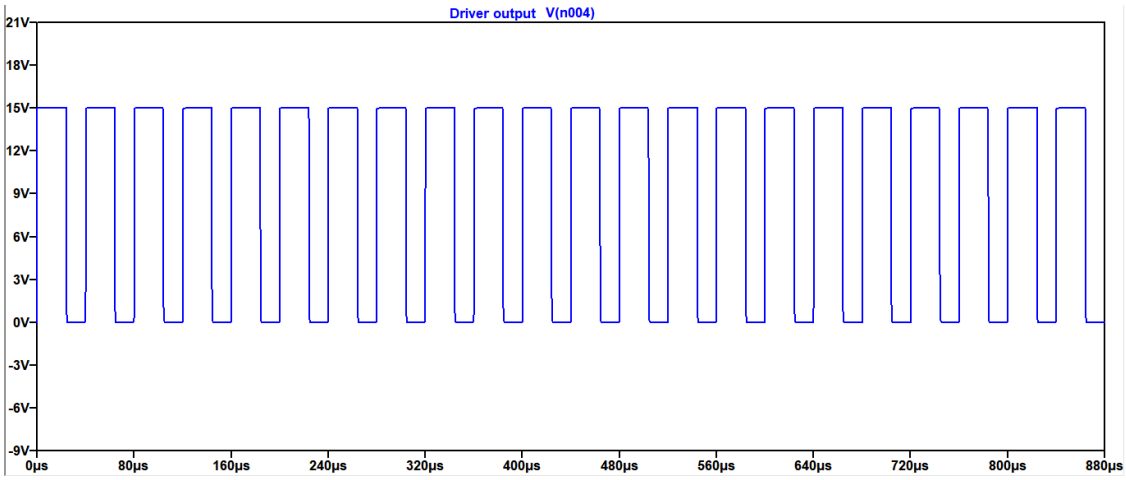


Fig. 2.19. Low side driver circuit output waveform

Advantage:

Handles the current spike and power losses very well.

Disadvantage:

The gate capacitances of N-channel and P-channel MOSFETs differ significantly. This mismatch in capacitance affects switching speed and can introduce timing issues.

2.8 CURRENT SENSOR

The current sensor is build using a differential amplifier [OPA192].

A differential amplifier consists of transistors, operational amplifiers, or a combination of both. Its primary function is to increase the voltage disparity between two input signals while disregarding any common-mode signals, which are signals present simultaneously on both inputs [25].

To sense current, a differential amplifier uses the voltage drop across a sensing resistor in series with the current path. The voltage across this resistor is proportional to the current passing through it, following Ohm's law (V = I * R).

The differential amplifier amplifies this voltage difference. The gain of the amplifier determines how much the output voltage changes concerning the change in input voltage.

This amplified voltage of the differential amplifier is converted into the actual current being sensed by multiplying it with a conversion factor.

2.8.1 Accuracy of the current sensor

The precision of the detecting resistor determines how accurate the current sensor is and the characteristics of the differential amplifier used.

Differential amplifier with high CMMR and low offset voltage is suitable for this application.

The amplifier used is OPA192 which is a high precision comparator used for high side current sensing. It has low offset voltage of ±5μv and high common mode rejection of 140 dB.

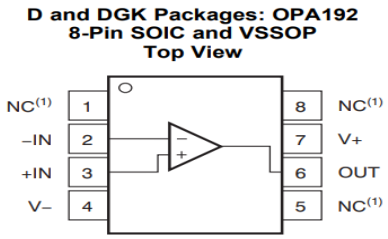


Fig. 2.21. Top view of OPA192 Differential Amplifier

2.8.2 CIRCUIT DIAGRAM

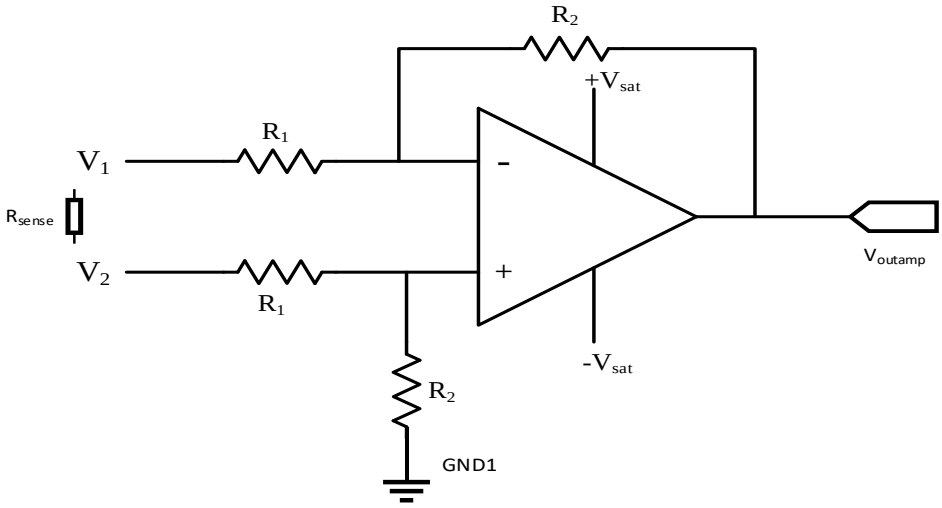


Fig. 2.22 Current sensor using Differential Amplifier

$$V_{outamp} = R_2/R_1*(V_2-V_1)$$

Table 2.4. Design Parameters for current sensor

Resistance(R_1)	10kΩ
Resistance(R_2)	100KΩ
$+V_{saturation}$	18v
$-V_{saturation}$	0v
Sensing Resistance(R_{sense})	33mΩ
Conversion factor	3.03
Current	V_{outamp}*3.03

2.9 CONCLUSION

The analysis of THD revealed that the Boost PFC Converter successfully drew sinusoidal current from the input source, leading to reduced harmonic distortion. By attaining a power factor nearing unity, the converter significantly improved power quality. A comprehensive assessment of THD and p.f under various load conditions offered a detailed understanding of how the converter operates, effectively reducing harmonics and correcting power factor issues.

The efficiency analysis provided insight into the energy conversion efficiency of the converter, factoring in losses occurring in switches, diodes, and other components. Assessing the cause of varying source voltage, output current, and switching frequency, this analysis offered substantial insights to optimize the operational efficiency of the converter. These findings present valuable guidance for improving the overall energy efficiency of AC-DC power supplies utilizing the Boost PFC Converter. The obtained efficiency of the converter is found to be 93.6%

In conclusion, this thesis has made a substantial contribution to comprehending the THD, efficiency, and overall performance of the Boost PFC Converter. The insights obtained from this thorough analysis establish a robust groundwork for future research and advancements in power factor correction and AC-DC power supply design. The knowledge derived from this thesis has the potential to drive progress in power electronics technologies, paving the way for more efficient and dependable power conversion systems.

CHAPTER 3
TOTEM-POLE PFC CONVERTER

3.1 INTRODUCTION

The Totempole PFC converter is a significant development in power electronics aimed at improving the effficiency and performance of power conversion circuits. With the increasing need for energy-efficient and reliable electrical systems, PFC converters are crucial for enhancing power factor correction, reducing harmonic distortions, and optimizing energy usage. This converter serves as a high-efficiency power converter used in AC-DC power supplies. Its innovative design combines advanced control methods and switching topologies to achieve superior power factor correction, ensuring efficient power transmission from the mains to the device. This architecture overcomes the limitations of traditional PFC circuits by minimizing losses and enhancing overall system efficiency [26]-[29]

This topology targets to improve traditional boost PFC converter designs by reducing losses and improving overall efficiency. The totem-pole boost converter removes the need for a diode bridge rectifier commonly used in conventional boost converters. By eliminating these diode bridge losses, the totem-pole boost converter reduces conduction losses and enables better utilization of the power available from the input source and higher efficiency, improved power factor and reduced component stress [30], [31].

3.2 CIRCUIT DIAGRAM

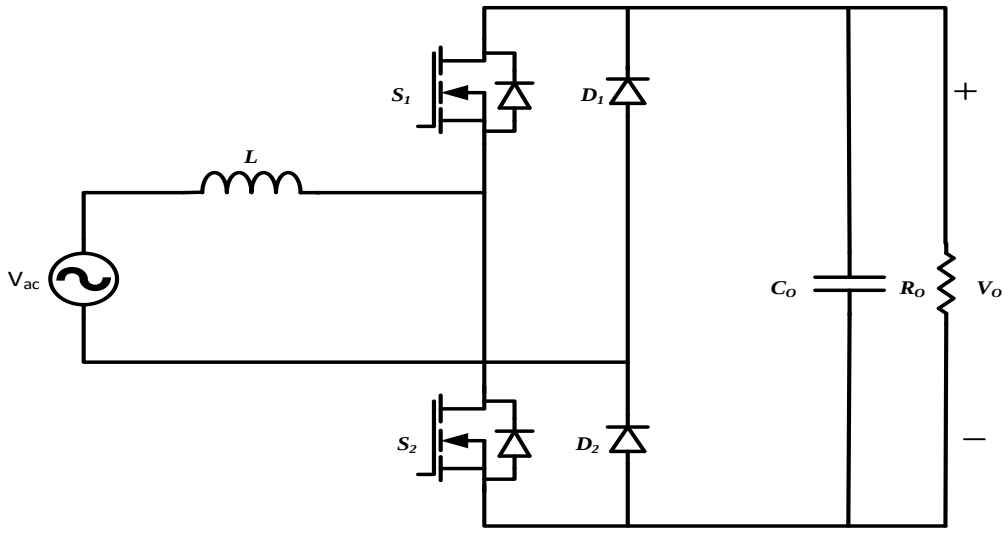


Fig. 3.1. Totem-Pole PFC Converter

3.3 OPERATION MODE ANALYSIS

Positive Half Cycle Operation

When the MOSFET S_2 is enabled, the load capacitor provides the energy to the load while coil L is charged by the input source. The input supply is connected to the output ground by the diode D_2, which is conducting.

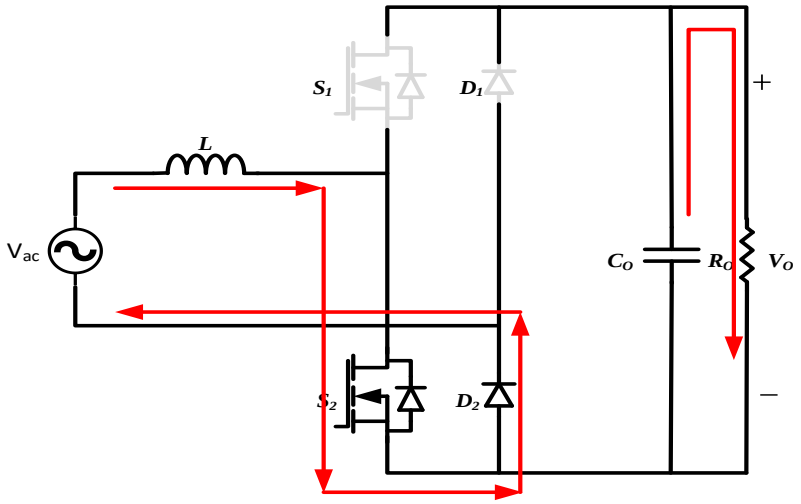


Fig. 3.2. Totem-Pole PFC when MOSFET S_2 is ON in positive supply

Additionally, when the Mosfet S_2 is disabled the coil L releases the energy to the load through MOSFET S_1 while the input is connected to the output ground by diode D_2, which is conducting.

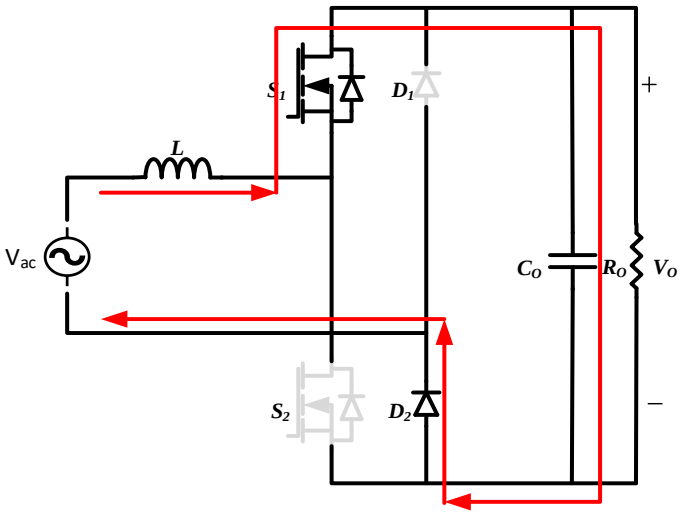


Fig. 3.3. Totempole PFC while MOSFET S_1 is ON in positive supply

Negative Half Cycle Operation

while the Mosfet S_1 is turned on, the input supply energises the coil L while the load capacitor provides load with energy. The Diode D_1 is forward biased and connects the input supply to the positive polarity of the output.

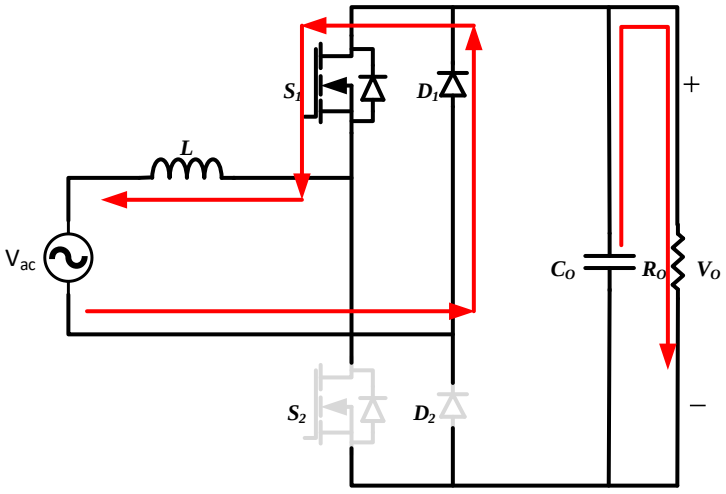


Fig. 3.4. Totem-Pole PFC when MOSFET S_1 is ON in negative supply

And while the Mosfet S_1 is deactivated, the coil L releases the energy to the load and Mosfet S_2 freewheels the current of the inductor. Diode D_1 conducts current, developing a connection between the source and the positive polarity of the load.

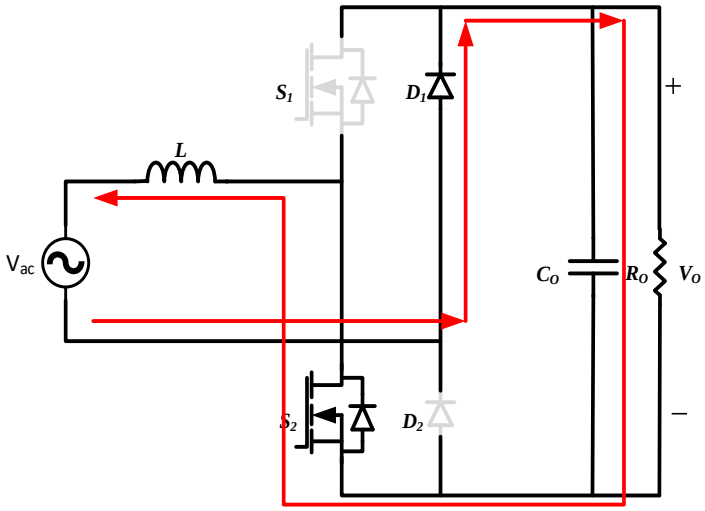


Fig. 3.5. Totempole PFC Negative cycle while MOSFET S_2 is ON

3.4 CLOSED LOOP CONTROL OF TOTEMPOLE PFC

In Totem-Pole PFC systems, the closed-loop control mechanism incorporates feedback loops that continually monitor vital parameters like input voltage, output voltage, input current, and occasionally additional variables such as temperature variations or load changes. These measured values are compared against reference values, enabling the control system to enact instantaneous modifications to the switching components (such as transistors). This dynamic process aims to uphold specified output voltage levels, regulate input current, and effectively achieve power factor correction [32].

The first phase begins by sensing the AC supply voltage to resemble a sinusoidal reference signal used by the current controller. Following this, a voltage regulator is utilized to manage the output voltage to get the reference current to which we want the inductor current to follow. The inductor current flows in opposite direction in every half cycle, so we use this logic to compare the inductor current with the

reference current and generate an error to be controlled by a PI controller. This controlled signal is converted into PWM for the respective switches.

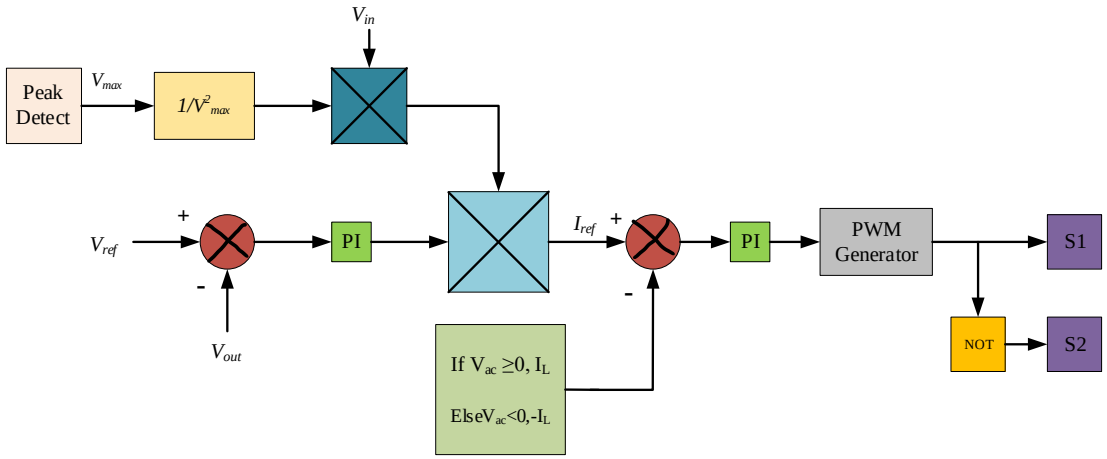


Fig. 3.6. Control of Totem-pole PFC

3.5 DESIGN OF TOTEM-POLE PFC CONVERTER

Table 3.1. Design specifications for totem-pole PFC

Supply (V_{in})	230 V
Load (V_o)	400 V
Power (P_o)	2500 W
Switching Frequency (f_{SW})	40kHz
Current Ripple (ΔI_L)	30%
Voltage Ripple (ΔV_c)	1% of output voltage
Load Resistance (R)	V_o^2/P_o
Inductor Resistance	60mΩ
ESR of Capacitor	40mΩ
Diode Forward Voltage drop	0.8 V
Diode On resistance	0.2 Ω
Mosfet On resistance	0.1 Ω
Inductor	330µH
Capacitor	4973µF

Additionally, to calculate the converters input inductor (L) and the output capacitor(C) we use the equations (1) and (2) respectively [3].

Inductor design

$$L = \frac{V_{in}^2}{\%Ripple * P_0 * f_{sw}} \left(1 - \frac{\sqrt{2} * V_{in}}{V_o}\right) \quad (1)$$

Capacitor Design

$$C_0 = \frac{P_0}{2\Pi * f_{line} * \Delta V_c * V_{bus}} \quad (2)$$

3.6 SIMULATION RESULTS

The totem-pole PFC Circuit is simulated using MATLAB software, and the outcomes are displayed in Fig. 3.7 and Fig. 3.8, presenting the waveforms of the input voltage and input current. As shown in fig. 3.9, the output voltage remains steady at 400V. Additionally, Fig. 3.11 showcases the characteristics of THD and fundamental current for the converter. For the proposed topology, an AC voltage of 230V was applied, and the inductor value was set at 330µH. The observation indicated synchronization between the load voltage and current of the configuration, signifying effective power factor correction. THD serves as a crucial performance metric, evaluating the quality of a power converter's output waveform.

INPUT VOLTAGE WAVEFORM

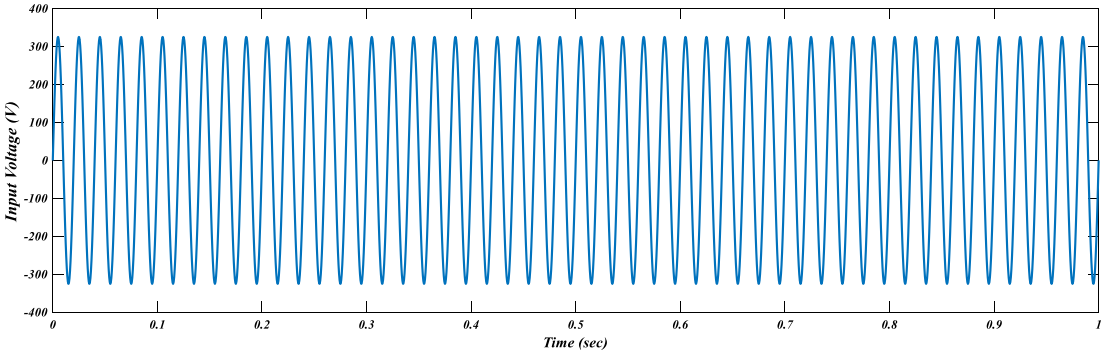


Fig. 3.7. Input voltage of Totem-Pole PFC

INPUT CURRENT WAVEFORM

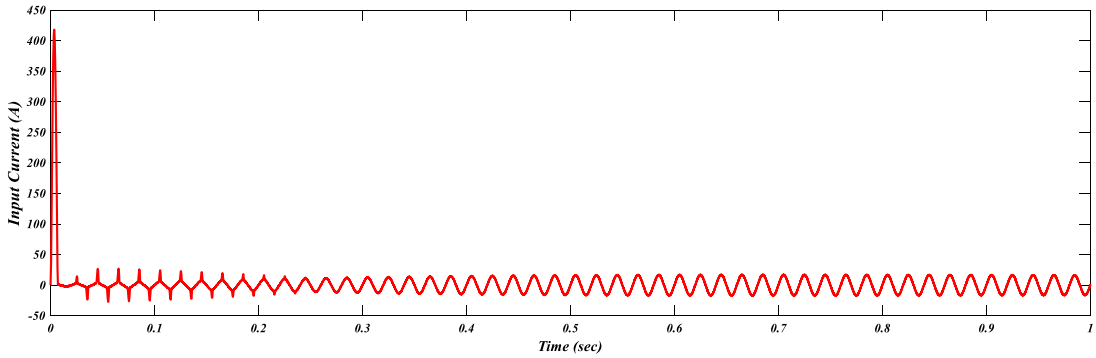


Fig. 3.8. Input current of Totem-Pole PFC

OUTPUT VOLTAGE WAVEFORM

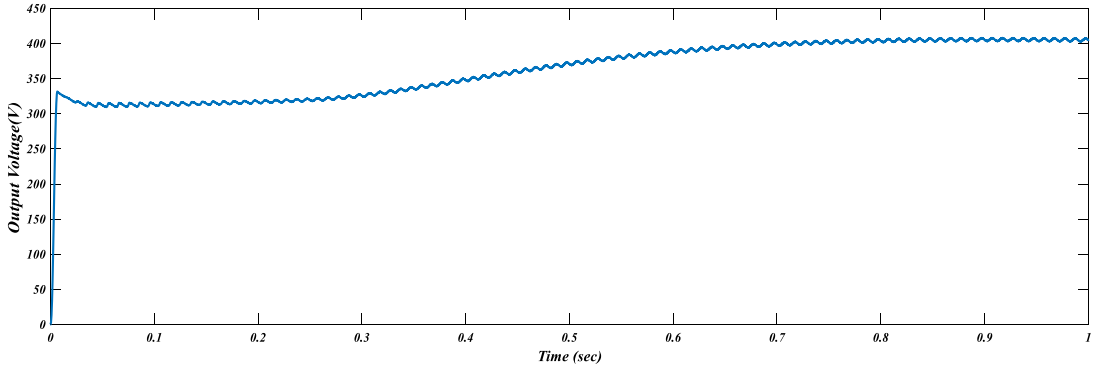


Fig. 3.9. Output voltage of Totem-Pole PFC

OUTPUT CURRENT WAVEFORM

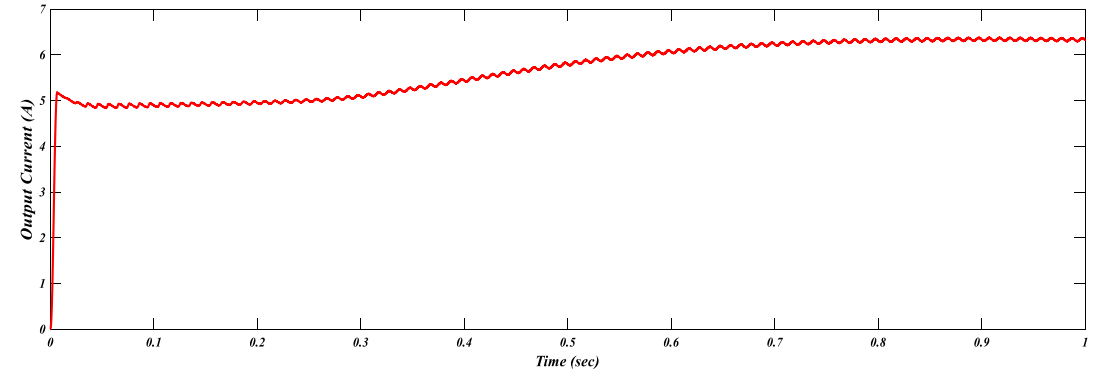


Fig. 3.10. Output current of Totem-Pole PFC

FFT ANALYSIS

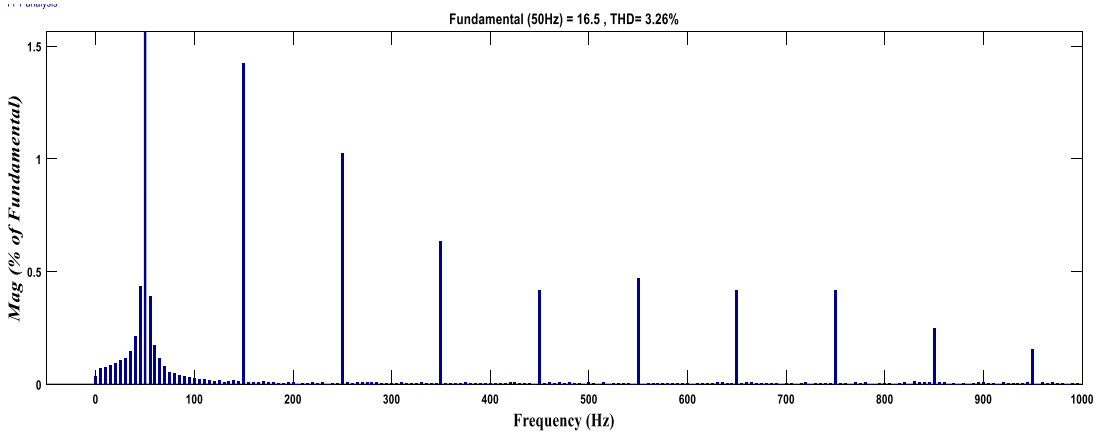


Fig. 3.11. FFT Analysis of Totem-Pole PFC

3.7 CONCLUSION

The detail of the THD indicates that the Totem-Pole PFC Circuit effectively drew sinusoidal current from the input source, resulting in reduced harmonic distortion. Achieving a p.f close to unity, the configuration notably enhanced power quality. The efficiency assessment provided a thorough understanding of energy conversion effectiveness within the converter, accounting for losses from switches, diodes, and additional components. By examining the impacts of varying input voltage, load current, and switching frequency, this analysis yielded significant insights to improve operational efficiency. These findings offer valuable guidance for enhancing the overall energy efficiency of AC-DC power supplies utilizing Totem-Pole PFC technology. The obtained efficiency of this converter is 95.64%.

In conclusion, the Totem-Pole PFC provides unity power factor, higher efficiency as well as improved THD as compared to Boost PFC.

CHAPTER 4

TOTEMPOLE PFC WITH MOSFET LINE RECTIFICATION

4.1 INTRODUCTION

This topology simply substitutes the line rectifiers D1 and D2 of the Totem-Pole PFC with switches S3 and S4, managed by two extra PWM circuits synchronized with the supply cycle.

Replacing diodes with MOSFETs in the Totem-Pole PFC architecture yields several advantages. MOSFETs, known for their lower forward voltage drop and reduced conduction losses compared to diodes, enhance efficiency and minimize power dissipation. This substitution effectively reduces losses typically associated with diode conduction in conventional PFC setups, optimizing input power utilization and improving overall system efficiency. Additionally, MOSFETs boast faster switching characteristics, enabling quicker turn-on and turn-off times. This feature helps reduce switching losses, leading to increased efficiency and providing better control over power flow within the system [27], [28].

Integrating MOSFETs into the Totem-Pole PFC design not only enhances efficiency but also enables more effective management of power flow, voltage regulation, and responsiveness to load fluctuations. These advancements are particularly significant in applications requiring high-efficiency power conversion, server energy supplies, EV charging circuits, sustainable energy converters, and industrial power equipment [33].

4.2 CIRCUIT DIAGRAM

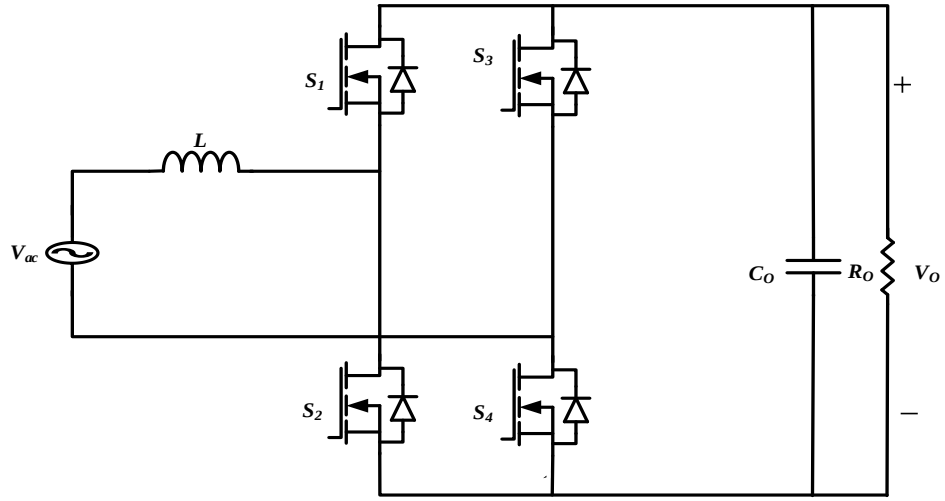


Fig. 4.1. Totem-Pole PFC with MOSFET line rectification

4.3 OPERATION MODE ANALYSIS

Positive Half Cycle Operation

while the Mosfet S_2 is enabled, the output capacitor provides the energy for the load while the coil L is energised by the input. The *AC* source is connected to the output ground by the Mosfet S_4, which is also on during this period.

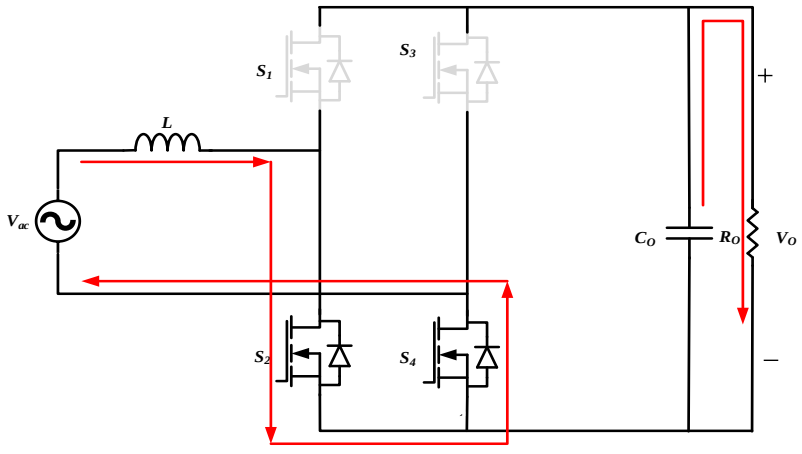


Fig. 4.2. Totem-pole PFC with mosfet line rectification when S_2, S_4 is ON

Additionally, when MOSFET S_2 is disabled the inductor *L* releases power to the load through the MOSFET S_1 while source is connected to the load negative by the Mosfet S_4, which is also on during this interval.

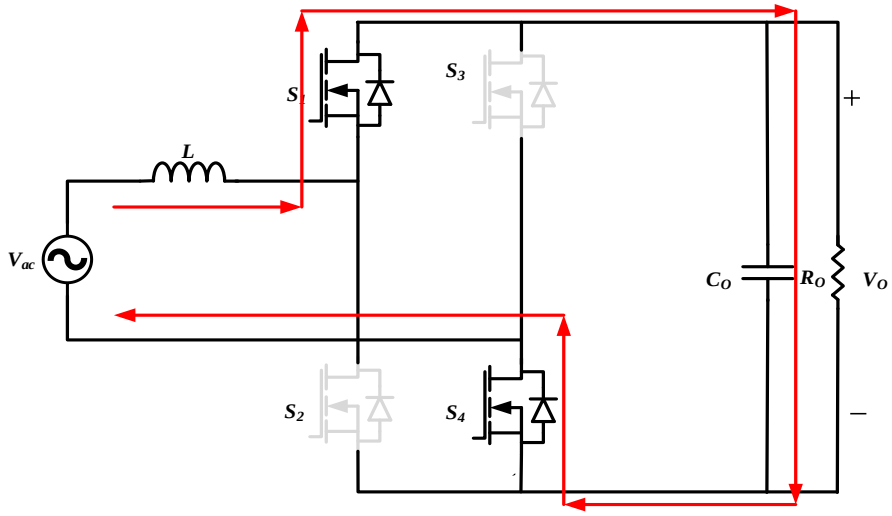


Fig. 4.3. Totempole PFC with mosfet line rectification while *S1*, *S4* is ON

Negative Half Cycle Operation

During negative half cycle of the input voltage, when the Mosfet S_1, S_3 are enabled, the input supply energises the coil *L* while the load capacitor provides the load with energy. The switch S_3 is conducting and connects the input supply to the positive terminal of the load.

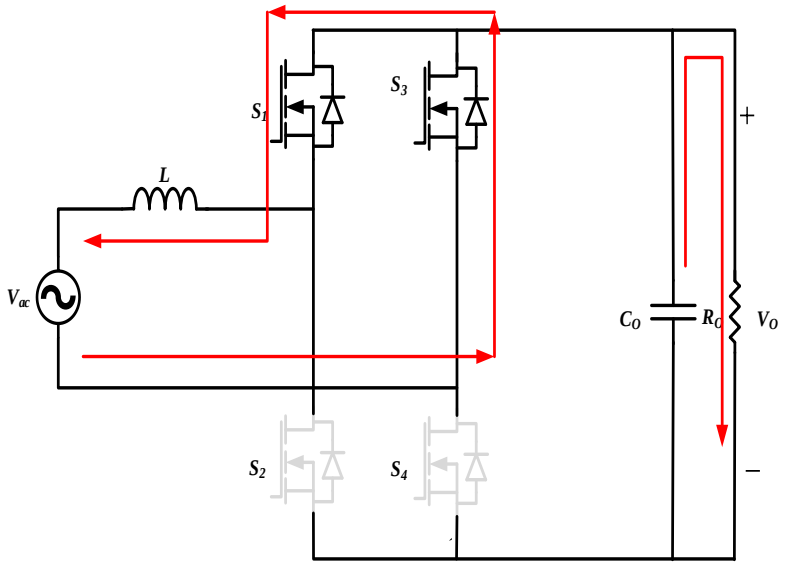


Fig. 4.4. Totem-Pole PFC with mosfet line rectification when S_1, S_3 is ON

And When the Mosfet S_1, S_4 are deactivated, the coil *L* releases the power to the output through Mosfet S_3 and freewheels the current through Mosfet S_2. The Mosfet

S_3 is connecting the ac source to the positive terminal of the output.

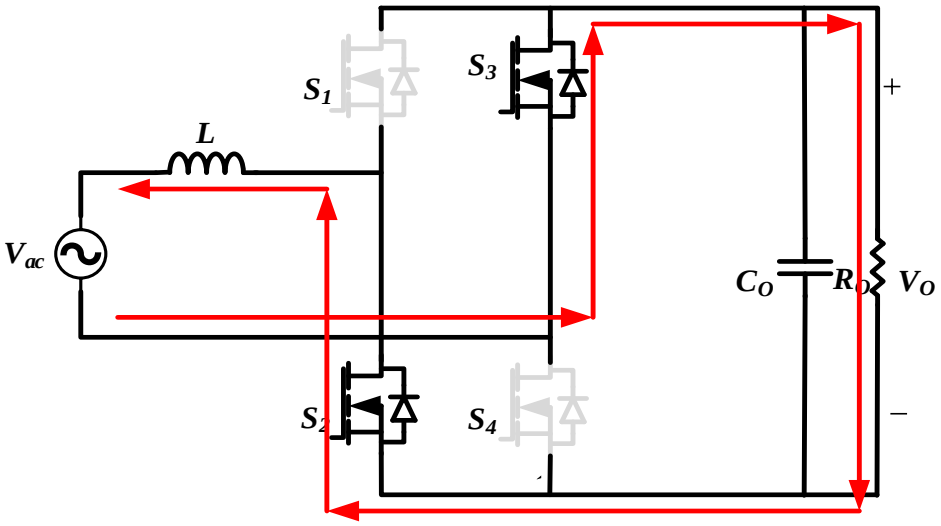


Fig. 4.5. Totem-pole PFC with mosfet line rectification while S_2, S_3 is ON

4.4 CLOSED LOOP CONTROL OF TOTEM-POLE PFC WITH MOSFET LINE RECTIFICATION

The first phase begins by sensing the AC supply to resemble a sinusoidal reference signal used by the current controller. Following this, a voltage regulator is utilized to manage the output voltage to get the reference current to which we want the inductor current to follow. The inductor current flows in opposite direction in every half cycle, so we use this logic to compare the inductor current with the reference current and generate an error to be controlled by a PI controller. This controlled signal is converted into PWM signal for the switch S1 and S2. Also, the switch S4 and S3 are switched ON during positive and negative cycle of the input voltage.

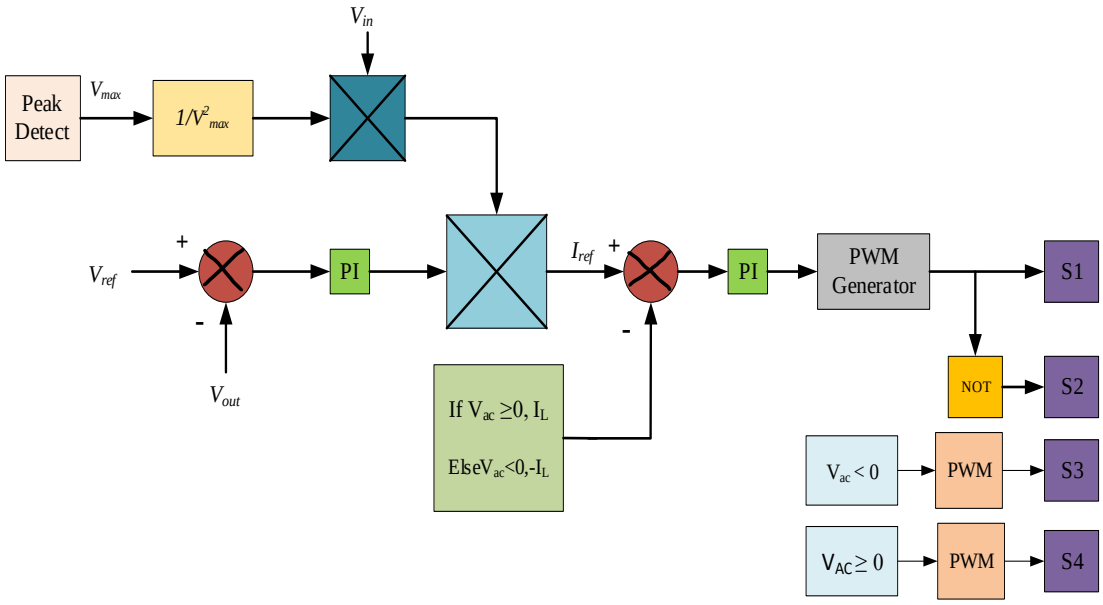


Fig. 4.6. Closed loop control of totem-pole PFC with mosfet line rectification

4.5 Design of Totem pole PFC with mosfet line rectification

Table 4.1. Design specifications for totem-pole PFC with MOSFET line rectification

Supply (V_{in})	230 V
Load (V_o)	400 V
Power (P_o)	2500 W
Switching Frequency (f_{SW})	40kHz
Current Ripple (ΔI_L)	30%
Voltage Ripple (ΔV_c)	1% of output voltage
Load Resistance (R)	V_o^2/P_o
Inductor Resistance	60mΩ
ESR of Capacitor	40mΩ
Diode Forward Voltage drop	0.8 V
Diode On resistance	0.2 Ω
Mosfet On resistance	0.1 Ω
Inductor	330µH
Capacitor	4973µF

Additionally, to calculate the converters input inductor (L) and the output capacitor(C) we use the equations (1) and (2) respectively [3].

Inductor design

$$L = \frac{V_{in}^2}{\%Ripple * P_0 * f_{sw}} \left(1 - \frac{\sqrt{2} * V_{in}}{V_o}\right) \quad (1)$$

Capacitor Design

$$C_0 = \frac{P_0}{2\Pi * f_{line} * \Delta V_c * V_{bus}} \quad (2)$$

4.6 SIMULATION RESULTS

To analyse the performance of the Totem-pole PFC with mosfet line rectification converter, a model was developed and simulated within the MATLAB environment.

Key waveforms, includes input voltage, input current, output voltage, output current and THD, were captured for analysis.

Input voltage waveform

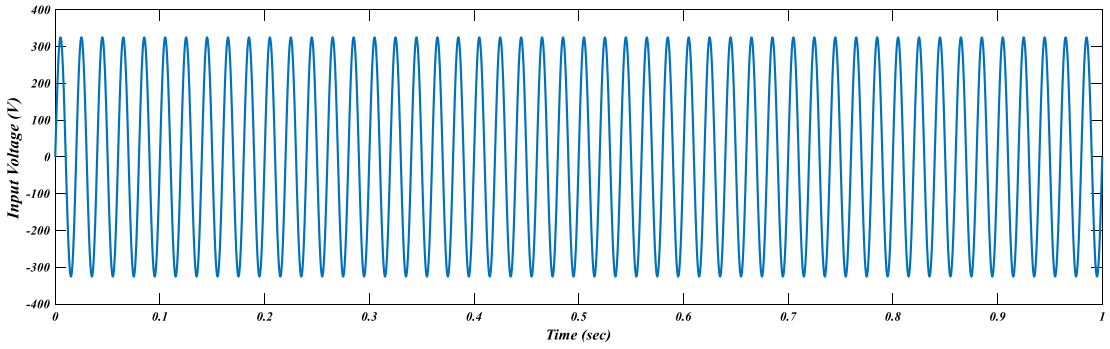


Fig. 4.7. Input voltage of totem-pole PFC with MOSFET line rectification

Input Current Waveform

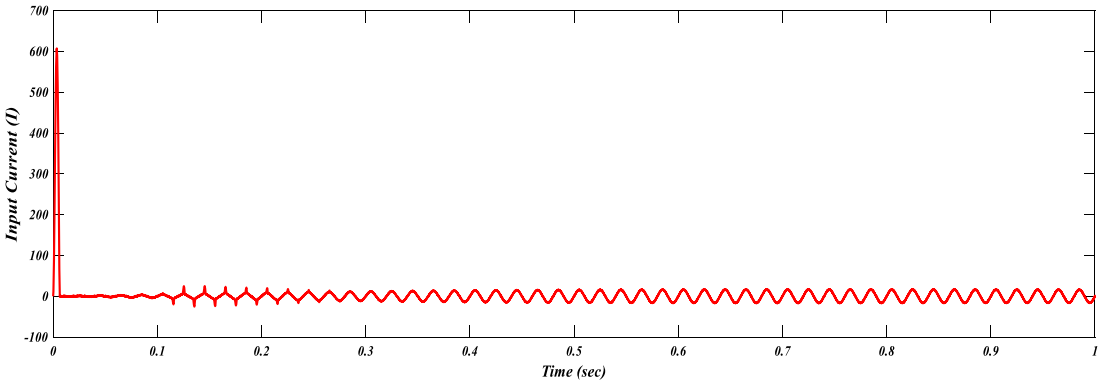


Fig. 4.8. Input current of totem-pole PFC with mosfet line rectification

OUTPUT VOLTAGE WAVEFORM

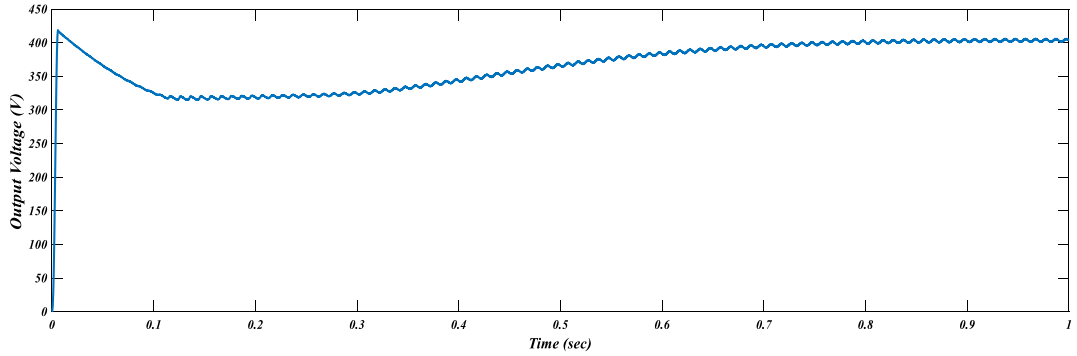


Fig. 4.10. Output voltage of totem-pole PFC with mosfet line rectification

OUTPUT CURRENT WAVEFORM

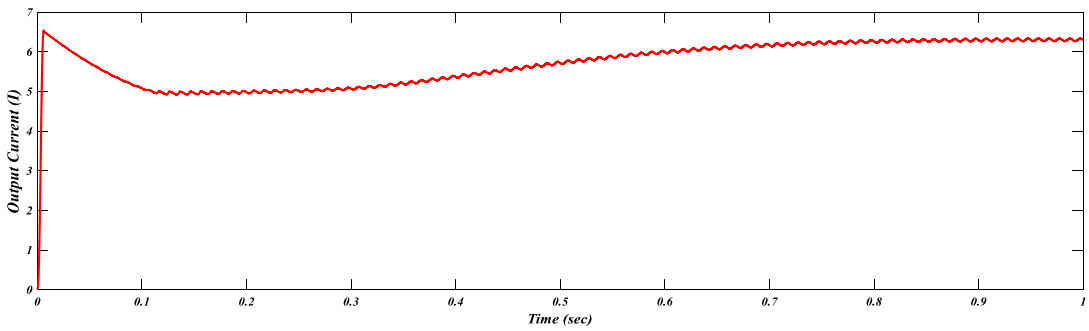


Fig. 4.11. Output current of totem-pole PFC with mosfet line rectification

FFT Analysis

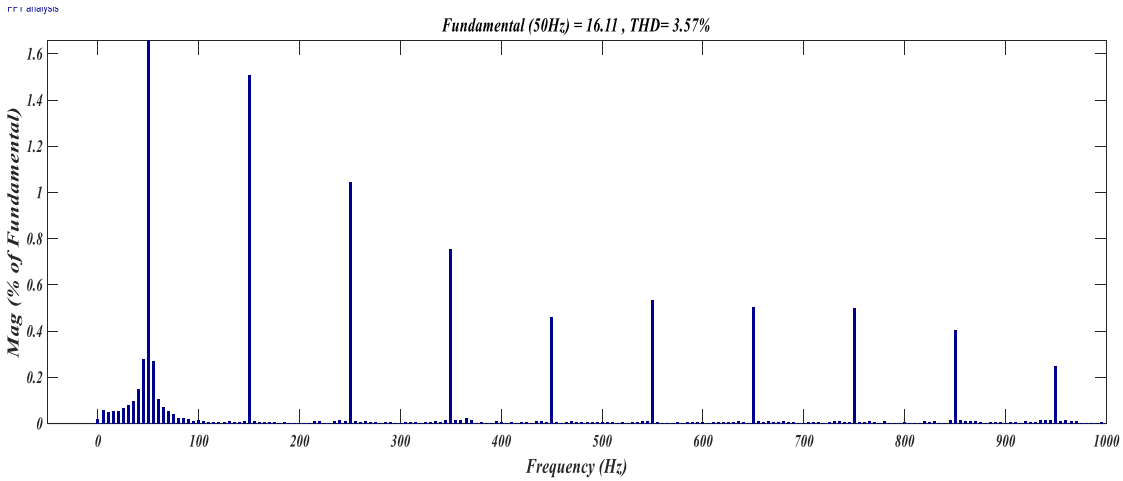


Fig. 4.12. THD of totem-pole PFC with mosfet line rectification

4.7 CONCLUSION

The analysis of THD indicated that the Totempole PFC with MOSFET line rectification effectively drew sinusoidal current from the AC source, resulting in reduced harmonic distortion. Achieving a pf close to unity, the configuration notably enhanced power quality. The efficiency examination provided a comprehensive understanding of the energy conversion effectiveness within the converter, considering losses from switches, diodes, and additional components. By assessing the impacts of varying input voltage, load current, and switching frequency, this analysis yielded significant insights to enhance the operational efficiency of the converter. These findings offer valuable guidance for improving the overall energy efficiency of AC-DC power supplies employing Totem-Pole PFC technology. The efficiency of the converter is obtained to be 97.16%.

In conclusion, this converter provides unity power factor and increased performance as compared to the Totempole PFC.

CHAPTER 5
INTERLEAVED TOTEMPOLE PFC

5.1 INTRODUCTION

The interleaved totempole PFC configuration is illustrated in Fig. 5.1. It consists of two inductor and six Si MOSFETs. The two boost interleaved phases (L_1, S_1, S_2 and L_2, S_3, S_4) operate with a phase displacement of 180 degrees. In each boost phases a deadband is provided between the complementarily high-side and low-side switches. Two-line rectification diodes are changed with MOSFETs (S_5 and S_6) for synchronous rectification [34]-[37].

5.2 CIRCUIT DIAGRAM

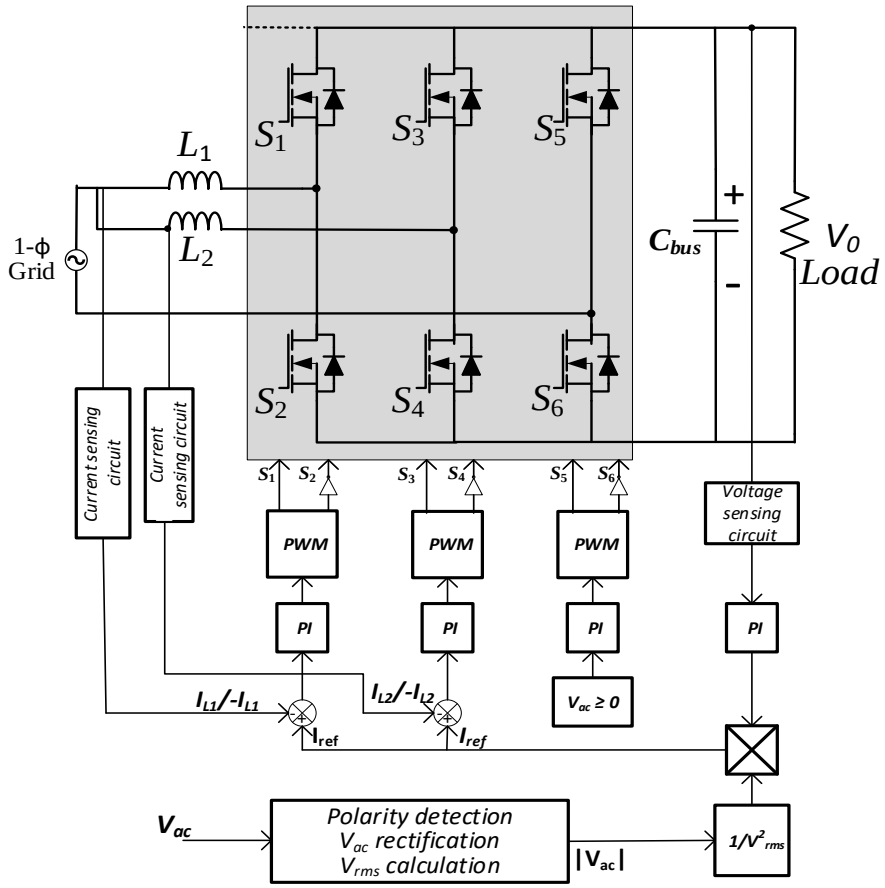


Fig. 5.1 Circuit and control diagram of interleaved totem pole PFC

5.3 OPERATION MODE ANALYSIS

Positive Half Cycle Operation

During positive half cycle of the input supply as depicted in Fig. 5.2, S_6 gets activated, linking the lower voltage of the input to the lower voltage of the output. As S_2 get enabled it results in a linear increase in the current flow through L_1.

$$\frac{di_{L_1}}{dt} = \frac{V_{ac}}{L_1} \qquad (5.1)$$

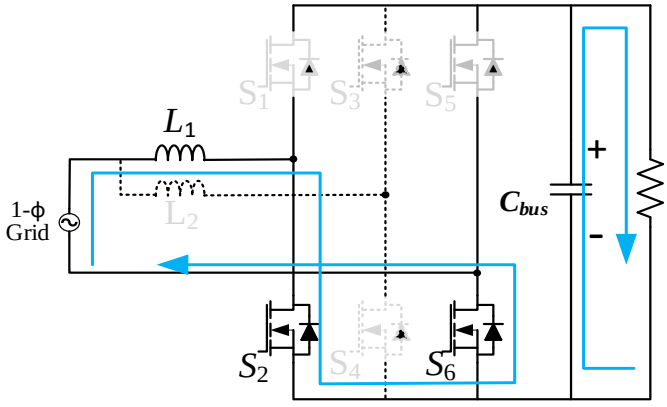


Fig. 5.2 Interleaved totem-pole PFC when S_2, S_6 is ON

Following the deactivation of S_2, a deadband interval is introduced before S_1 is activated to prevent the surge current. After this deadband period, as illustrated in Fig. 5.3, S_1 is triggered, establishing a way for the inductor current to dissipate to the output bus. Consequently, there is a linear drop in the current passing through L_1.

$$\frac{di_{L_1}}{dt} = \frac{V_{ac} - V_{bus}}{L_1} \qquad (5.2)$$

.

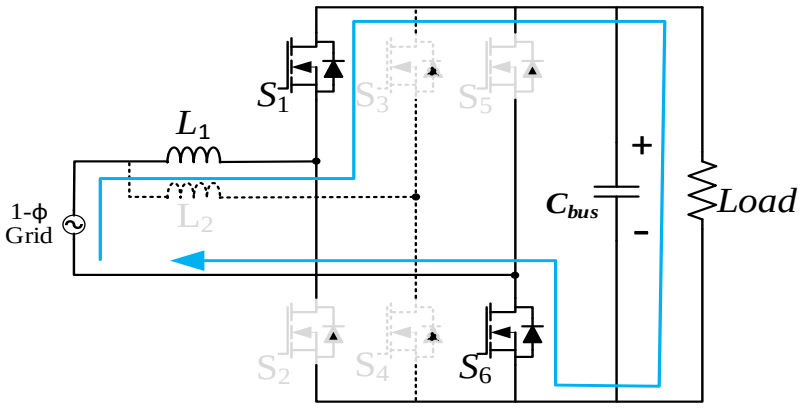


Fig. 5.3 Interleaved totem-pole PFC when S_1, S_6 is ON

Negative Half Cycle Operation

During the negative half-cycle, S_5 is activated, establishing a connection between the input supply and the load. As depicted in Fig. 6.4, when S_1 is triggered, the input supply energises the coil L_1, resulting in a linear increase in current as per (1). Subsequently, S_2 is activated after S_1 is deactivated, introducing a deadband interval to facilitate synchronous rectification. This action creates a freewheeling path for the inductor current, as illustrated in Fig. 6.5. Consequently, the flow of current through inductor reduces uniformly according to (2).

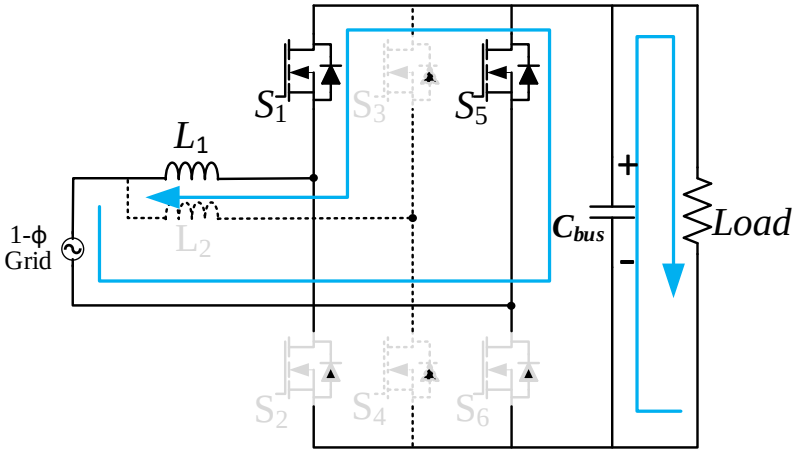


Fig. 5.4 Interleaved Totem-Pole PFC when S_1, S_3 is ON

And When the Mosfet S_1, S_4 are deactivated, the coil L releases the power to the output by Mosfet S_3 and freewheels the current through Mosfet S_2. The Mosfet S_3 is connecting the supply to the positive node of the output.

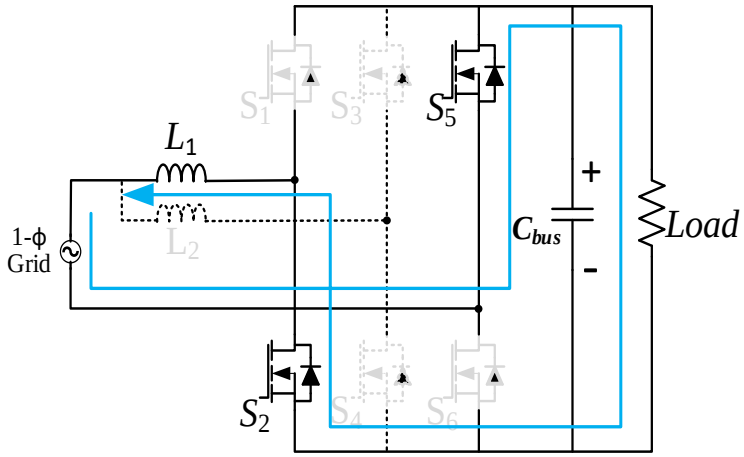


Fig. 5.5 Interleaved Totem-Pole PFC when S_2, S_5 is ON

5.4 CLOSED LOOP CONTROL OF INTERLEAVED TOTEMPOLE PFC WITH MOSFET LINE RECTIFICATION

Control of the Interleaved Totempole PFC converter is displayed in Fig.6.1, it begins by sensing the supply to resemble a sinusoidal reference signal used by the current controller. Following this, a voltage regulator is utilized to manage the output voltage to get the reference current to which we want the inductor current to follow. Each inductor currents are compared with this reference current and generate an error to be controlled by the PI controllers. This controlled signal is converted into PWM signal for the switch S_1, S_2 and S_3, S_4. Also, the switch S_5 and S_6 are switched ON during positive and negative cycle of the input voltage.

5.5 Design of Interleaved Totem-pole PFC

Table 5.1. Design specifications for interleaved totem-pole PFC

Supply (V_{in})	230 V
Load (V_o)	400 V
Power (P_o)	2500 W
Switching Frequency (f_{SW})	40kHz
Current Ripple (ΔI_L)	30%
Voltage Ripple (ΔV_c)	1% of output voltage
Load Resistance (R)	V_o^2/P_o
Inductor Resistance	60mΩ
ESR of Capacitor	40mΩ
Diode Forward Voltage drop	0.8 V
Diode On resistance	0.2 Ω
Mosfet On resistance	0.1 Ω
Inductor	330µH
Capacitor	2486µF

Additionally, to calculate the converters input inductor (L) and the output capacitor(C) we use the equations (1) and (2) respectively [3].

Inductor design

$$L = \frac{V_{in}^2}{\%Ripple * P_0 * f_{sw}} \left(1 - \frac{\sqrt{2} * V_{in}}{V_o}\right) \quad (1)$$

Capacitor Design

$$C_0 = \frac{P_0}{4\Pi * f_{line} * \Delta V_c * V_{bus}} \quad (2)$$

5.6 SIMULATION RESULTS

To analyse the performance of Interleaved totempole PFC with mosfet line rectification converter, a model was developed and simulated within the MATLAB environment.

Key waveforms, includes input voltage, input current, output voltage, output current and THD, were captured for analysis.

Input voltage waveform

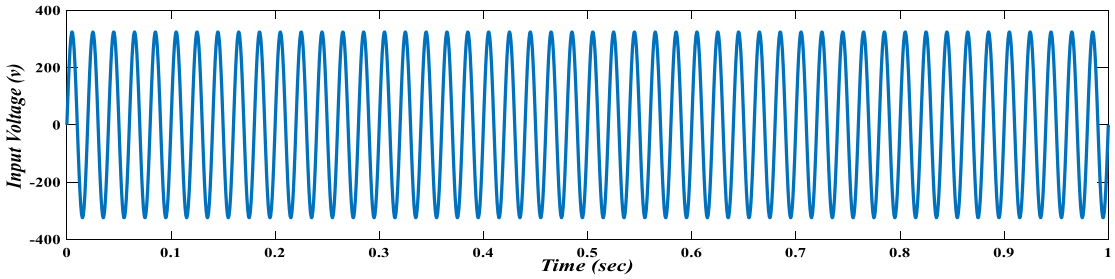


Fig. 5.6 Input voltage of Interleaved totempole PFC

Input Current Waveform

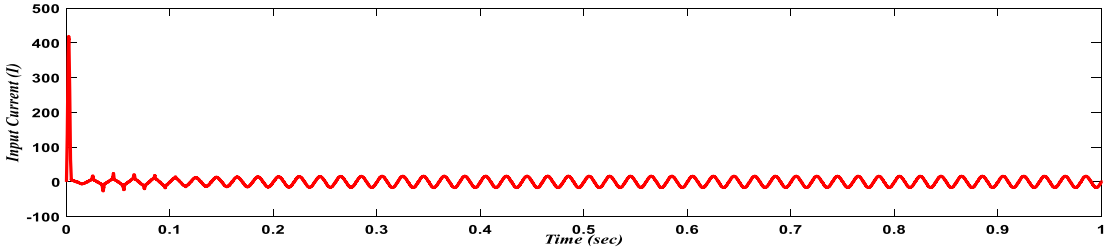


Fig. 5.7 Input current of Interleaved totempole PFC

OUTPUT VOLTAGE WAVEFORM

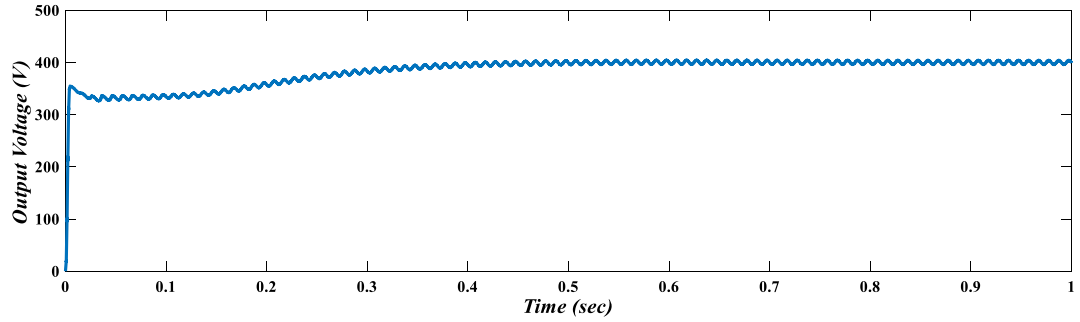


Fig. 5.9 Output voltage of Interleaved totem-pole PFC

OUTPUT CURRENT WAVEFORM

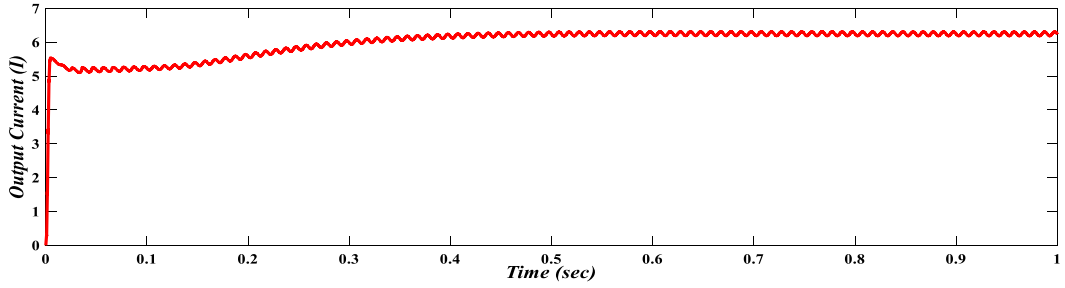


Fig. 5.10 Output current of Interleaved totem-pole PFC

FFT Analysis

Fast Fourier Transform (FFT) analysis of the Interleaved totem-pole PFC with mosfet line rectification is done using MATLAB/SIMULINK and the THD of the input current is found to be 4.75% shown in Fig. 14. i.e. harmonic is less than 5% of fundamental.

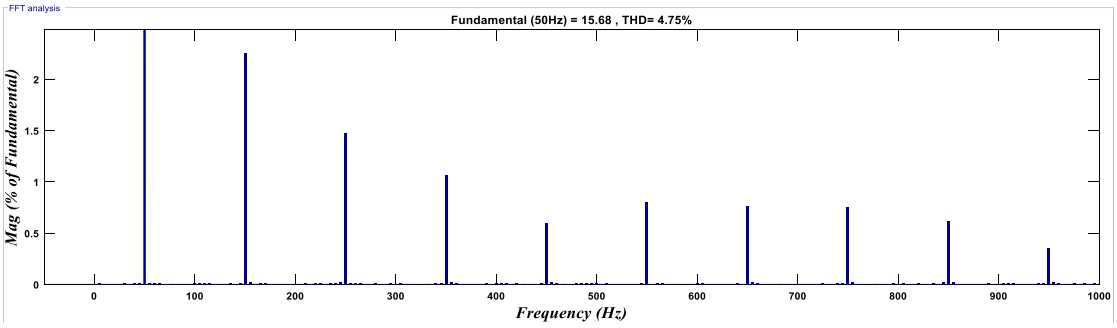


Fig. 5.11 THD of Interleaved totem-pole PFC with mosfet line rectification

5.7 CONCLUSION

The analysis of THD revealed that the Interleaved totem-pole Power Factor Correction Converter successfully drew sinusoidal current from the AC source, leading to reduced harmonic distortion. By attaining a power factor nearing unity, the converter significantly improved power quality.

The efficiency analysis provided a thorough understanding of the energy conversion effectiveness within the converter, taking into account losses from switches, diodes, and additional components. By evaluating the impacts of input voltage, load current, and switching frequency, this analysis yielded significant insights to improve the operational performance of the configuration. These results offer valuable guidance for enhancing the overall energy efficiency of AC-DC power supplies utilizing Interleaved Totem-Pole PFC technology. The efficiency of the converter is obtained to be 97.92%.

In conclusion, the Interleaved totem-pole PFC provides unity power factor and increased performance as compared to the other configuration.

CHAPTER 6

DESIGN AND ANALYSIS OF A 4KW INTERLEAVED TOTEMPOLE PFC BASED ON-BOARD CHARGER USING PSFB DC-DC CONVERTER

6.1 INTRODUCTION

This chapter investigates the performance analysis of an on – Board charger (OBC), designed to charge a lithium-ion battery used in an electric vehicle. The complete diagram of the designed system is depicted in Fig. 6.1. It includes two stages of power conversion in which the first stage consists of an interleaved totem-pole based PFC converter to convert the ac grid voltage into DC voltage without polluting the grid current and the second stage consists of a PSFB DC-DC converter to control the charging of the battery cells, while providing isolation between the grid and the battery. It explains the fundamental working principle, governing equations and closed loop control of both the stages. The input is fed from grid whose voltage variation range is considered as (200-250) V AC, 50Hz and it is converted to 400V DC bus by the start stage and the end stage consists of a high frequency step-down transformer for charging a lithium-ion battery rated at 48V/60 Ah. MATLAB/Simulink is utilized to validate the outcomes of the developed OBC. The findings contribute to the progression of on-board charging technology, thereby improving the sustainability and convenience of electric vehicles (EVs).

6.2 CIRCUIT DIAGRAM

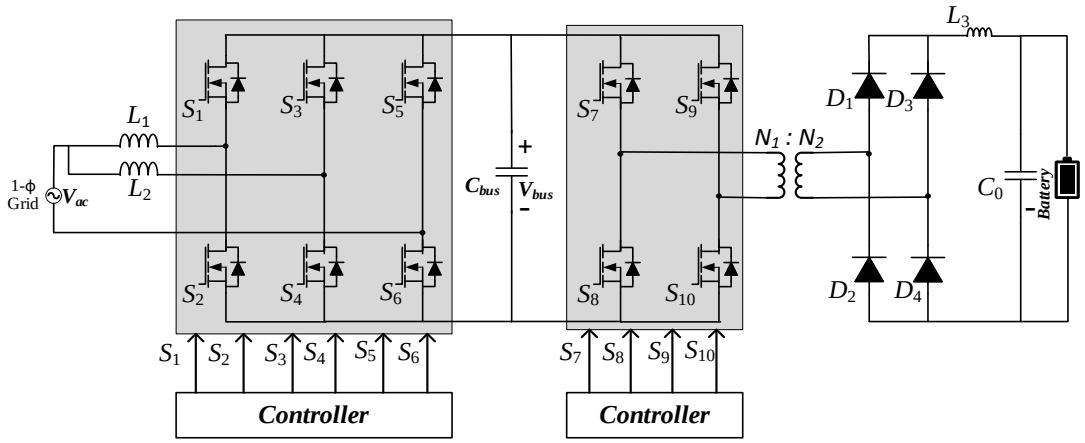


Fig. 6.1 On-board Charger using interleaved totempole PFC and PSFB converter

6.3 SYSTEM DESCRIPTION

6.3.1 Interleaved Totempole PFC converter

The interleaved totempole PFC converter is illustrated in Fig. 6.2. It consists of two inductor and six Si MOSFETs. The two boost interleaved phases (L_1, S_1, S_2 and L_2, S_3, S_4) operate with a phase displacement of 180 degrees. In each boost phases a deadband is provided between the complementarily high-side and low-side switches. Two-line rectification diodes are changed with MOSFETs (S_5 and S_6) for synchronous rectification. Circuit and control diagram of interleaved totempole PFC converter is shown in fig. 5.1

Control of the Interleaved Totempole PFC converter is shown in Fig. 2, it begins by sensing the AC supply to resemble a sinusoidal reference signal used by the current controller. Following this, a voltage regulator is utilized to manage the output voltage to get the reference current to which we want the inductor current to follow. Each inductor currents are compared with this reference current and generate an error to be controlled by the PI controllers. This controlled signal is converted into PWM signal for the switch S_1, S_2 and S_3, S_4. Also, the switch S_5 and S_6 are switched ON during positive and negative cycle of the input voltage.

Table 6.1. Design specifications for the font end PFC circuit

PFC Parameter	**Value**
Grid Voltage (V_{ac})	(200-250)V_{rms}
Output Voltage (V_{bus})	400V
Grid Frequency (f_{line})	50Hz
Switching Frequency (f_{SW})	80kHz
Power (P_o)	4kW
Inductor Current Ripple (ΔI_L)	10%
Output Voltage Ripple (ΔV_c)	3%

6.3.2 Phase Shifted Full Bridge DC-DC Converter

PSFB DC-DC converter is frequently utilized for the purpose of stepping down high DC voltages to lower levels by employing a transformer which also ensures isolation between the supply and the battery [37]-[39]. The circuit diagram of PSFB Converter is depicted in Fig. 6.3. It has a 400V DC supply at the input and four switches which helps the high frequency transformer to transfer energy to the output side and provide the required gain. To limit the charging current ripple, an inductor is utilized while a capacitor is used to filter and regulate the output voltage [40]-[42].

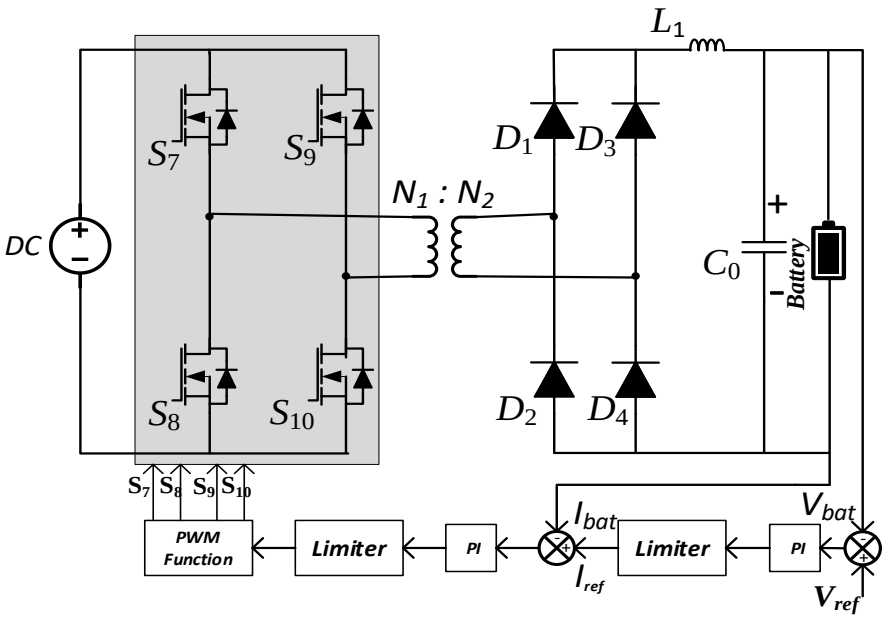


Fig. 6.3. Circuit and Control diagram of PSFB DC-DC converter

Table 6.2. Design specifications for the phase shifted full bridge dc-dc converter

PSFB Parameter	**Value**
Supply DC voltage	400V
Load Battery voltage	48V
Turns Ratio (N_S/N_P)	0.27
Power	4kW
Switching Frequency	50kHZ
Inductor Ripple (ΔI_L)	10%
Capacitor Ripple (ΔV_c)	1%
Inductor	130 µH
Capacitor	68 µF

The circuit diagram of the closed-loop control for a PSFB converter is presented in Fig. 6.3. The controller features a current and voltage control loop. The maximum

voltage of the battery is 55V(V_{ref}). To restrict the battery charging current to its maximum value (37.5A), a limiter is installed at the voltage controller's output. In order to restrict the maximum PWM phase shift to 180 degrees, a limiter is additionally included at the current controller's output [44]-[45].

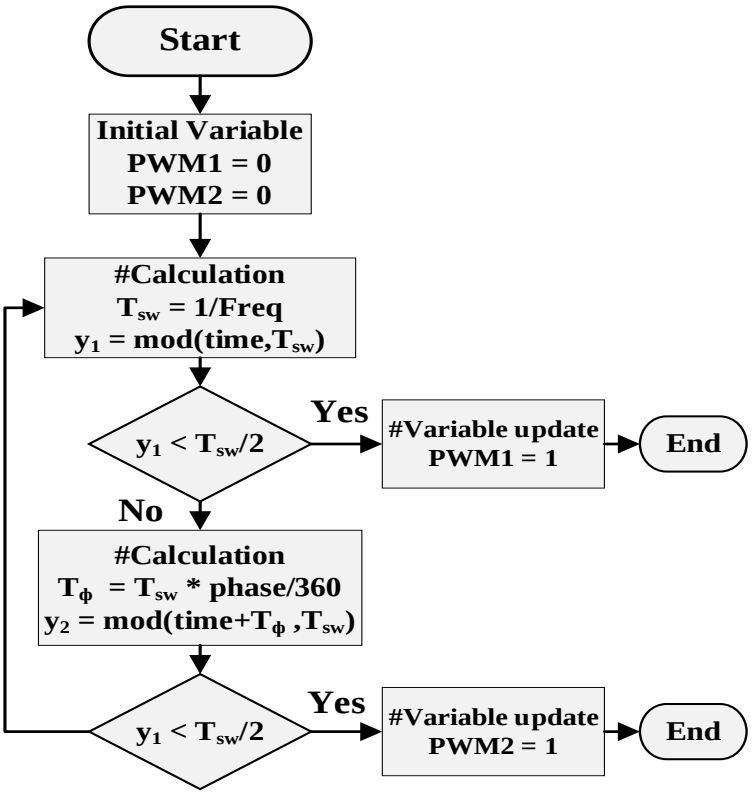


Fig. 6.4. Control algorithm for the PWM function of the PSFB converter.

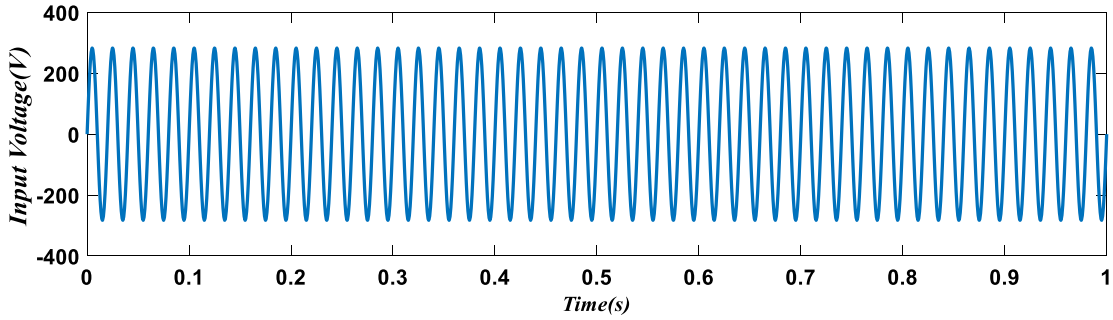
The control algorithm of the PWM function block in Fig. 6.3 is explained by the flowchart in Fig. 6.4. Here PWM1 is used to control the switched S_7 & S_{10} and PWM2 is used to control the switches S_8 & S_9. PWM1 turns S_7 & S_{10} on when mod (time, T_{sw}) is less than half of the switching period and PWM2 turns S_8 & S_9 on when mod (time+ phase shift, T_{sw}) is less than half of the switching period [43].

6.4 SIMULATION RESULTS

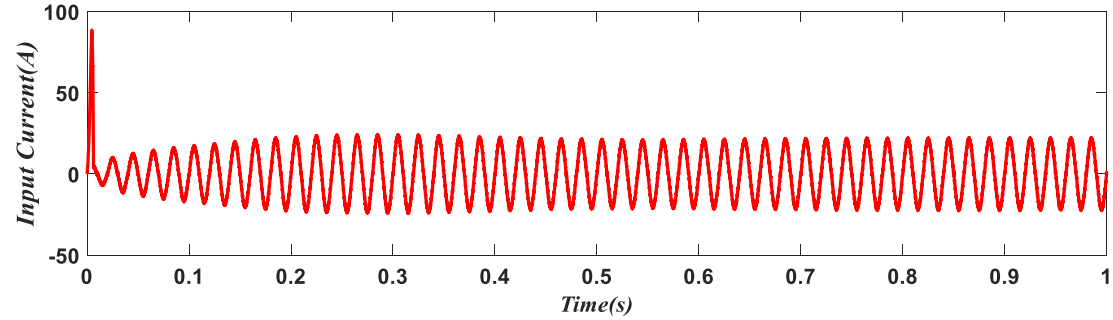
MATLAB/Simulink is used to validate the 4kW On-board charger as shown in Fig. 1. Here different grid voltage is applied to the input of the interleaved totem-pole PFC and maintained a DC bus voltage of 400V for the PSBF converter to charge a 48V/60Ah lithium-ion battery.

For the effectiveness of the OBC the grid voltage is considered at 200V, 230V and 250V rms voltage and validation is done by checking the IPF, DC bus voltage for the PFC converter and current, voltage, SOC (%) of the battery for the PSFB DC-DC converter [46]-[47].

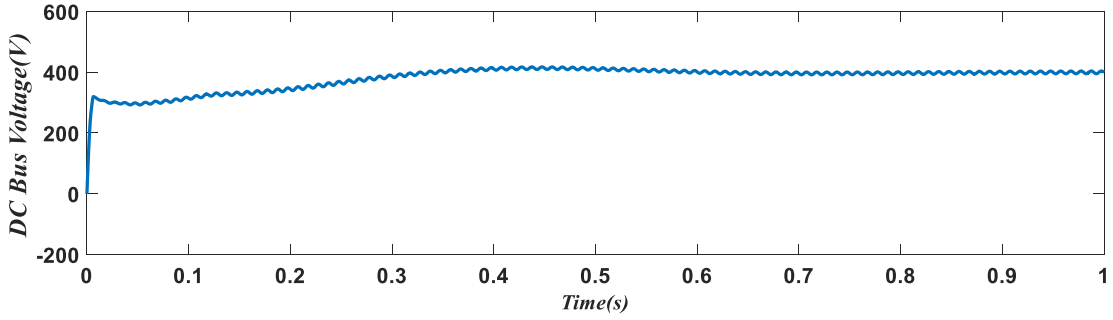
1) For 200V rms grid voltage



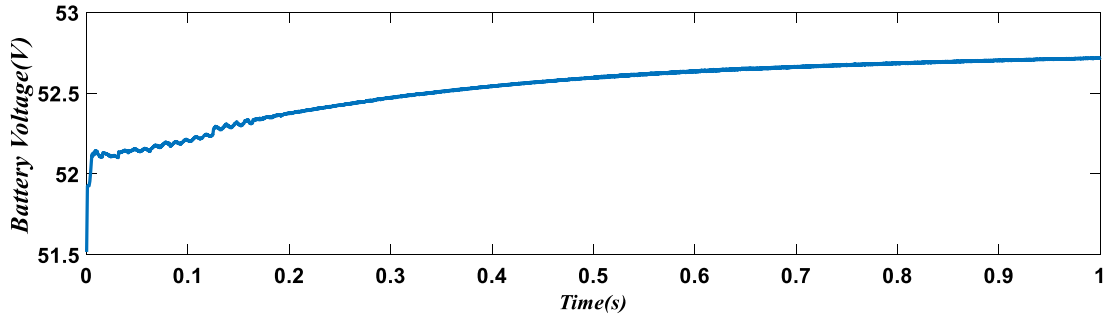
(a)



(b)



(c)



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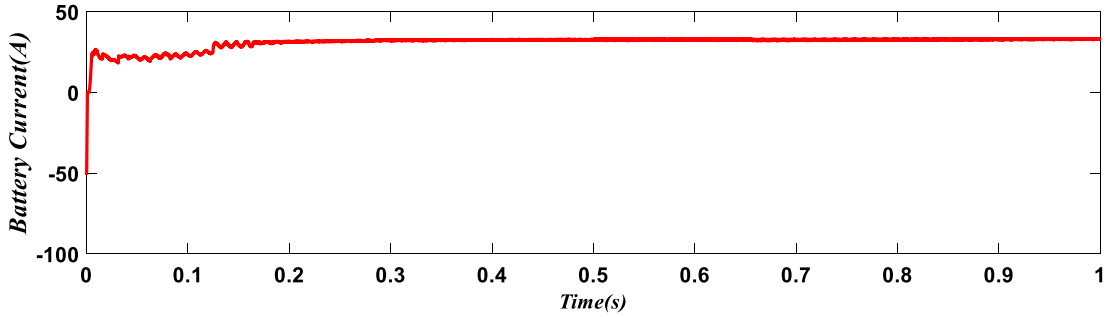

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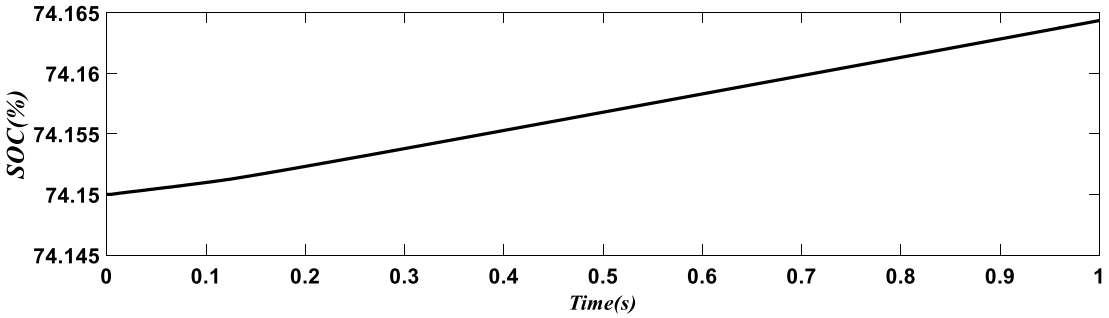

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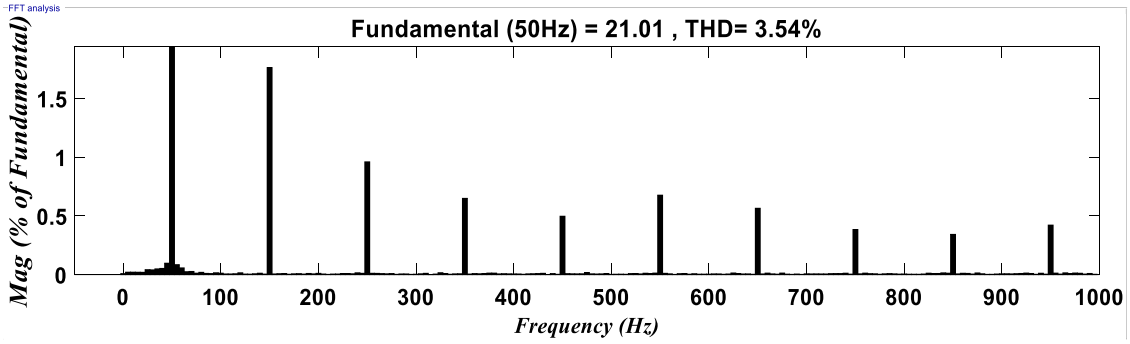
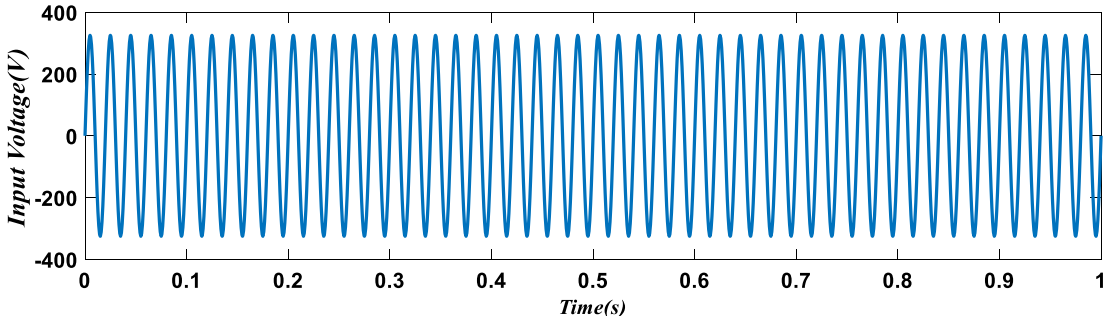


(g)

Fig. 6.5. Simulation results for the OBC at 200V rms grid voltage (a) Supply voltage (b) Supply current (c) DC bus voltage (d) Battery voltage (e) Battery current (f) SOC (%) of the battery (g) THD of the grid current.

1) For 230V rms grid voltage



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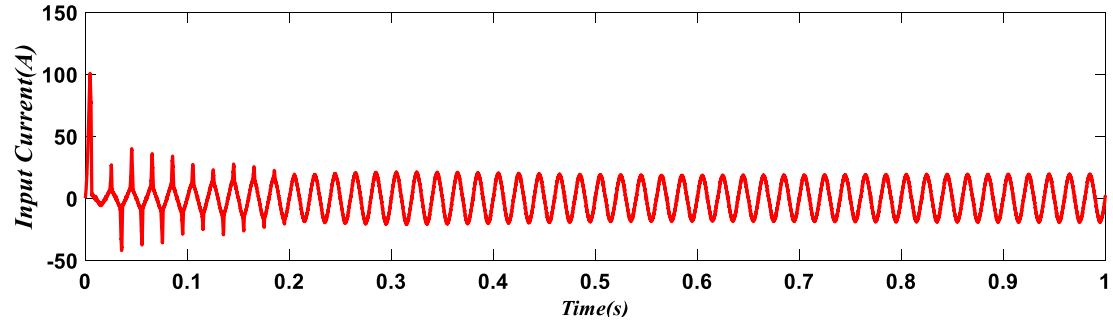

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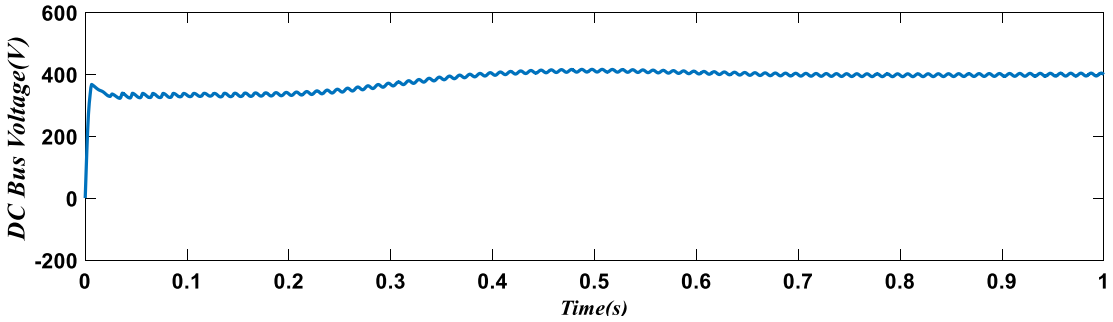

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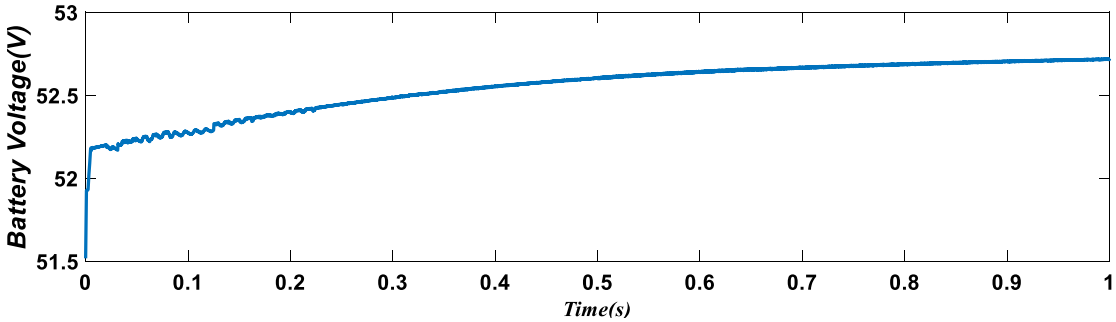

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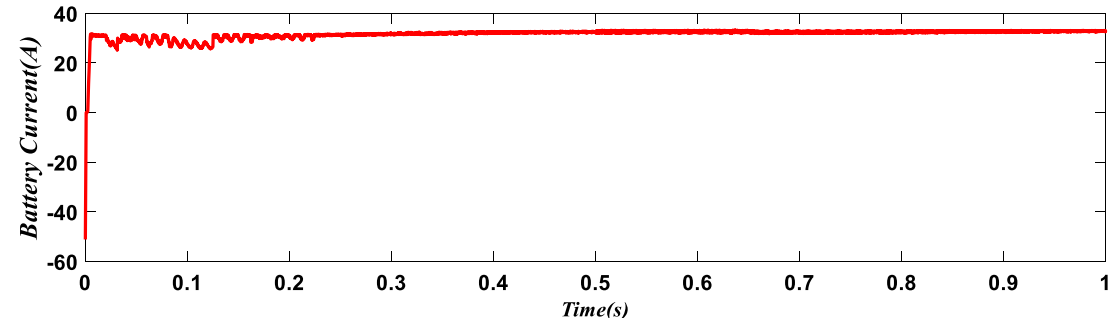

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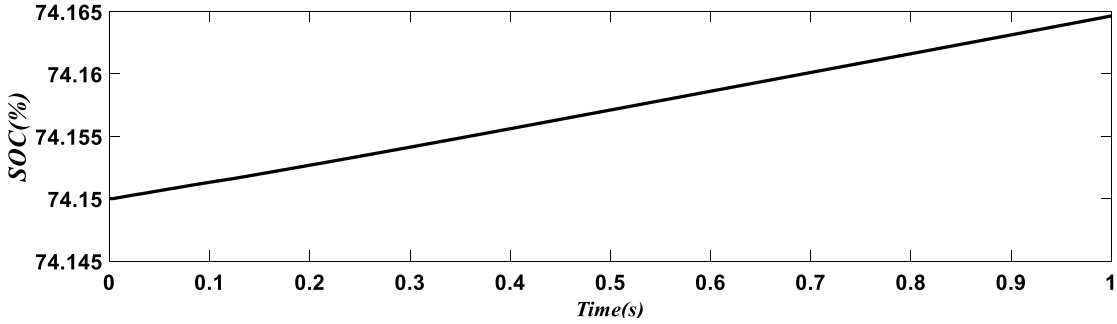
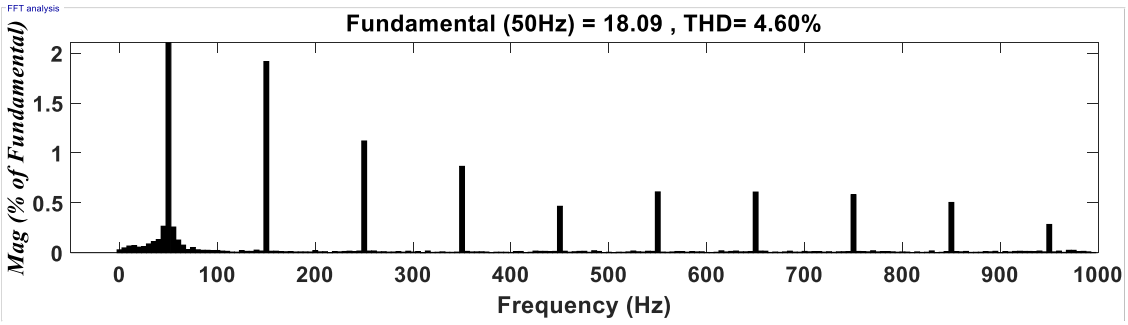


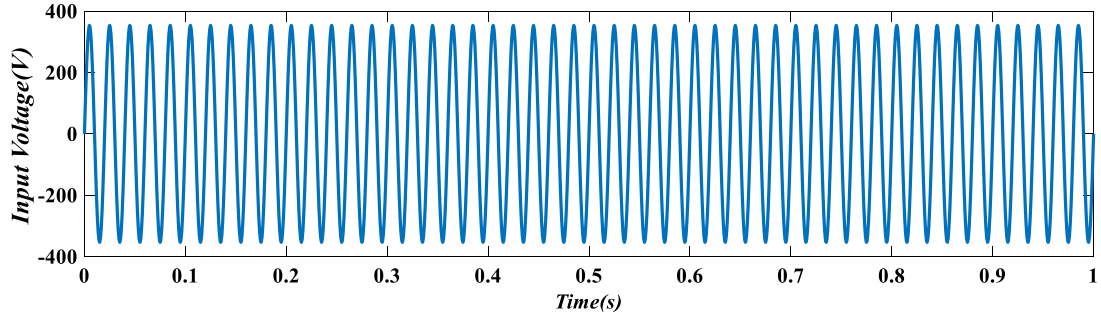
(f)



(g)

Fig. 6.6. Simulation results for the OBC at 230V rms grid voltage (a) Supply voltage (b) Supply current (c) DC bus voltage (d) Battery voltage (e) Battery current (f) SOC (%) of the battery (g) THD of the grid current.

2) For 250V rms grid voltage



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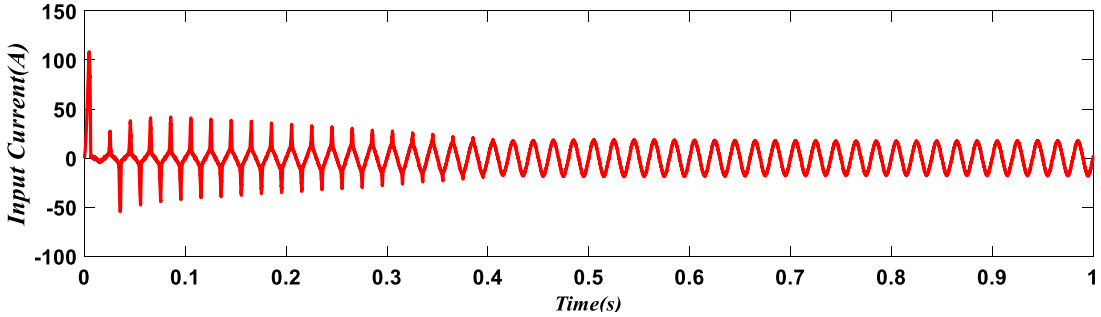

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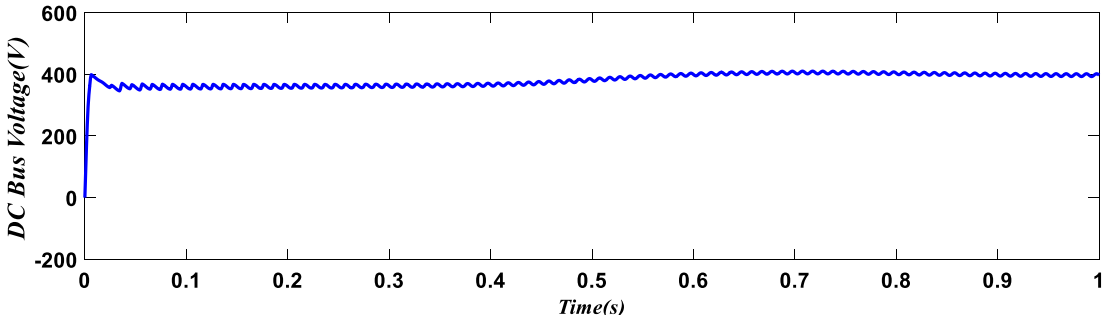

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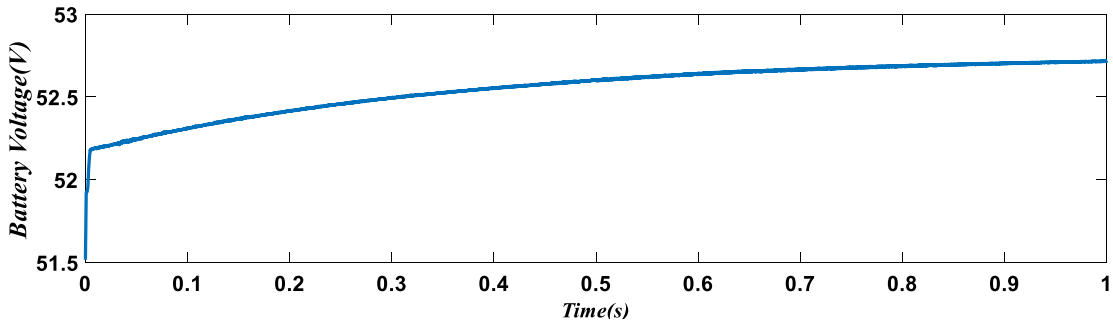

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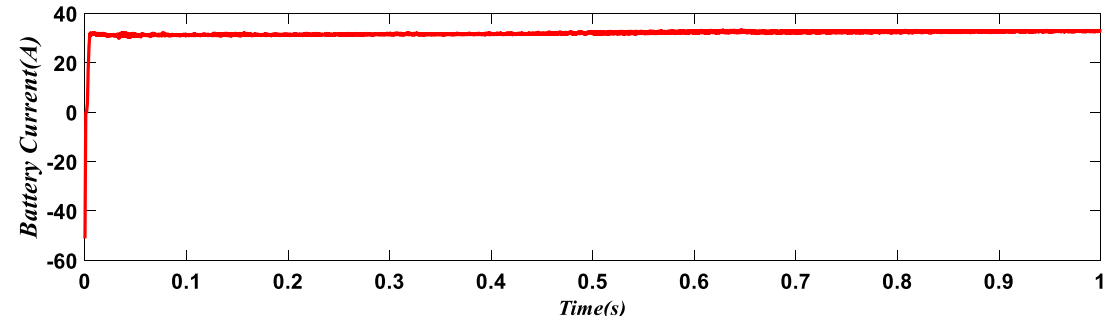

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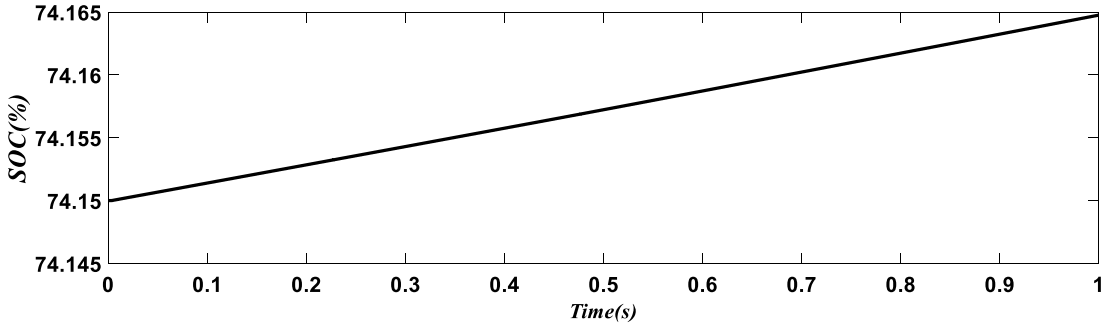
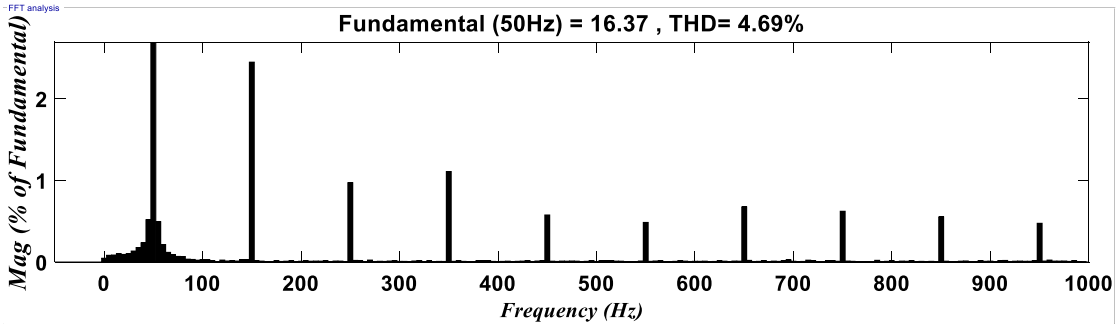


(f)



(g)

Fig. 6.7. Simulation results for the OBC at 250V rms grid voltage (a) Supply voltage (b) Supply current (c) DC bus voltage (d) Battery voltage (e) Battery current (f) SOC (%) of the battery (g) THD of the grid current.

From the fig. 6.5(a),6.6(a) and 6.7(a) it can be seen that the grid has a sinusoidal rms voltage of 200V, 230V and 250V and the grid current is shown in figure 6.5(b),6.6(b) and 6.7(b) which has a varying magnitude of the current spike at the respective voltages. For 200V rms grid voltage the grid current has the THD of 3.54% while for 230V and 250V the THD's are 4.60% and 4.69% as shown in fig. 6.5(g),6.6(g) and 6.7(g). In all the three cases the THD is reduced to less than 5%

and a DC bus voltage of 400V is sustained as shown in fig. 6.5(c),6.6(c) and 6.7(c), hence verifying the working of the PFC converter. While the second stage PSFB DC-DC converter can charge the lithium-ion battery as the battery voltage shown in fig. 6.5(d),6.6(d) and 6.7(d) and SOC shown in fig. 6.5(f),6.6(f) and 6.7(f) keeps on increasing due to the constant current supplied by the PSFB converter as shown in fig. 6.5(e),6.6(e) and 6.7(e), thus the performance of both the stage validates the overall effectiveness of the OBC.

6.5 CONCLUSION

This chapter discusses the performance analysis of a 4kW two-stage OBC intended for charging a lithium-ion battery rated at 48V/60Ah. All the systems were designed to ensure efficient charging of the battery and maintaining the input current in phase with the input voltage. In the first stage, the interleaved totem-pole PFC circuit is designed to reduce the THD to less than 5%, achieving near unity PF and capable of sustaining a 400V bus voltage. In the second stage, the switching algorithm of the PSFB converter was designed in such a way that the output voltage is suitable to charge the lithium-ion battery. All findings and discussions are verified through MATLAB-Simulink simulations and comprehensively presented with in this chapter.

CHAPTER 7
CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

The comparison between Boost PFC, Totem-Pole PFC, Totem-Pole PFC with mosfet line rectification and Interleaved totem-pole PFC showcases a clear evolution in balancing efficiency, power factor correction, and complexity.

- **Boost PFC**: The basic Boost PFC converter topology consists of a diode, inductor, capacitor, and a switch. It provides improved power factor correction by regulating the input current. It is simple and cost-effective but limited in efficiency (93.6%) due to diode bridge rectifier and suffers from higher current ripple and a slightly lower power factor (0.99).
- **Totem-Pole PFC**: The totem-pole Boost PFC converter employs a push-pull configuration with two active switches replacing the diode bridge rectifier. It provides improved efficiency and reduced conduction losses. A significant leap in efficiency (95.64%), reduces size and EMI, but requires a complex control circuit.
- **Totem-Pole PFC with MOSFET line rectification**: This topology integrates MOSFETs instead of diodes in the line rectification of the Totem-Pole PFC architecture. MOSFETs, distinguished by their lower forward voltage drop and reduced conduction losses compared to diodes, offer heightened efficiency and minimized power dissipation. By replacing diodes with MOSFETs, it achieves unrivalled efficiency (97.16%), and delivers the THD of less than 5%. This superior efficiency translates to lower operational costs and reduced environmental impact. Additionally, the active control over MOSFETs grants finer power flow management, precise voltage regulation, and improved responsiveness to load changes.
- **Interleaved Totem-Pole PFC**: It consists of two inductor and six Si MOSFETs. The two boost interleaved phases operate with a phase difference of 180 degrees. In each boost phases a deadband is provided between the

complementarily high-side and low-side switches. Two-line rectification diodes are replaced with MOSFETs for synchronous rectification. It has higher power handling capability, lower input and output current ripple and improved efficiency (97.92)% compared to other PFC topologies but has a higher component count, higher cost and design complexity compared to other PFC topologies.

While the added complexity of the Interleaved Totem-Pole PFC might pose a slight hindrance in some scenarios, its unparalleled efficiency, power factor correction, and dynamic control capabilities make it the ultimate choice for applications demanding the best performance.

7.2 FUTURE SCOPE

Key Areas for Advancement:

1. Wider Adoption and Increased Efficiency:
    - Streamline integration of PFC techniques across diverse applications, spanning consumer electronics, industrial drives, and renewable energy systems.
    - Prioritize research on topologies and control strategies that maximize efficiency, minimizing energy losses and enhancing cost-effectiveness.
2. Advanced Topologies and Control:
    - Explore innovative PFC topologies that address current limitations, such as: Bridgeless PFC with reduced conduction losses and enhanced reliability. Interleaved bridgeless PFC for higher power handling capabilities and reduced ripple currents. Soft-switching PFC techniques for improved efficiency and reduced EMI.
3. Using SiC and GaN devices in the PFC topologies for wider range of application.

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LIST OF PUBLICATIONS

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