A DISSERTATION ON

Implementation of Half Adder Using Recessed Channel MOSFET Based on Mixed-Mode Simulation

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BHARAT CHOUDHARY

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UNDER THE SUPERVISION OF

Dr. RISHU CHAUJAR

Assistant Professor

DEPARTMENT OF ENGINEERING PHYSICS

DELHI TECHNOLOGICAL UNIVERSITY

DELHI -110042

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CERTIFICATE

This is to certify that the dissertation entitled "***Implementation of Half Adder Using Recessed Channel MOSFET Based on MixedMode Simulation***" submitted by **Mr. Bharat Choudhary** in the partial fulfillment of the requirement for the award of the degree of M.Tech. in Nano Science and Technology from the Department of Applied Physics, Delhi Technological University, Delhi is a record of candidate's own work carried out by him under my supervision.

Dr. Rishu Chaujar
Supervisor
Assistant Professor, (ENGG. Physics Dept.)
Delhi Technological University

Prof. S. C. Sharma
HOD
Dept. of Applied Physics
Delhi Technological University

DECLARATION BY THE CANDIDATE

I hereby declare that the work presented in this dissertation entitled "**Implementation of Half Adder Using Recessed Channel MOSFET Based on MixedMode Simulation**" has been carried out by me under the guidance of **Dr. Rishu Chaujar**, Assistant Professor of Engineering Physics department, Delhi Technological University, Delhi and hereby submitted for the partial fulfillment for the award of degree of Master of Technology in Nano Science and Technology at Applied Physics Department, Delhi Technological University, Delhi.

I further undertake that the work embodied in this major project has not been submitted for the award of any other degree elsewhere.

Bharat Choudhary

2K11/NST/02

M.Tech (NST)

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Bharat Choudhary

M.Tech (NST)

2K11/NST/02

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ABSTRACT

We observe that in the past few decades the minimum size of transistor has been downscaled according to the Moore's law. But now further downscaling of MOSFET is facing challenges like SCE(short channel effects), gate insulator tunneling. To overcome these challenges Recessed Channel MOSFET, a type of grooved device, is the most promising device structure.

RC-MOSFET technology has the caliber to continue with the Moore's law. RC-MOSFET has started replacing conventional MOSFETs. RC-MOSFET is a non planar structure in which the drain and source regions are separated from one another through a groove, the extension of the drain electric field toward the channel region is restrained. The presence of groove minimizes the SCEs and punch through effects, thereby enhancing the hot-carrier reliability.

This thesis work analyses the implementation of Half Adder circuit using RC-MOSFET based on MixedMode simulation and also analyses through literature survey the effects of variation in various device parameters like drain current(I_{on}), threshold voltage(V_t), DIBL and subthreshold swing(S), impact ionization of RC-MOSFET by using simulation tools 3D Silvaco ATLAS version5.16.3.R and Devedit version 2.6.0.R.

Chapter 1

MOSFET FUNDAMENTALS

1.1 Introduction of MOSFET

MOSFET is the most widely used electronic device, particularly for Integrated Circuits. More than 99% of all ICs are MOSFETs used for random-access-memory, flash memory, processors, ASICs (application-specific integrated circuits), and other applications. The structure of the MOS field-effect transistor (MOSFET) has two regions of doping opposite that of the substrate, one at each edge of the MOS structure as shown in **Figure 1.1**.These regions are called the source and drain, and a pn junction exists between them and substrate. When terminals are connected to all the various regions of the MOSFET, a four terminal device results, with the terminal designate as G (gate), S (source), D (drain) and B (substrate).

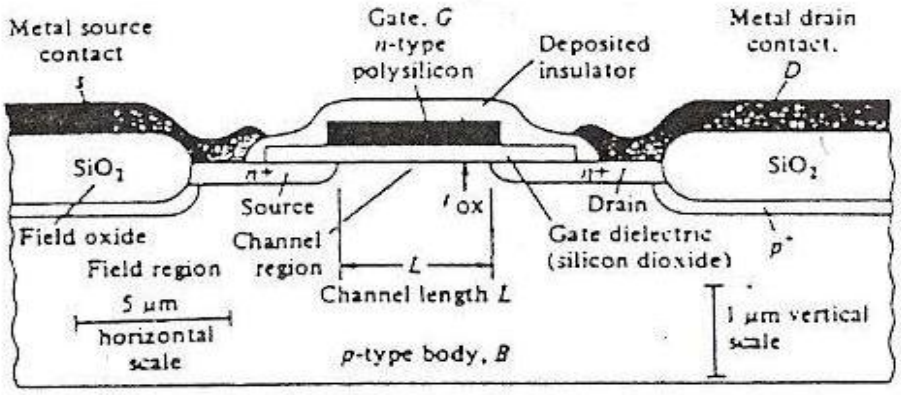


Figure 1.1: *Structure of MOS device [11]*

Since one of these terminals can be designated as the common terminal, three independent terminal voltages can be applied to the MOSFET. However, only one significant current exists in an ideal MOSFET. That is, we assume that the gate current is zero ($I_G = 0$) and that the source and drain junctions are always kept under reverse bias during normal MOSFET operation. Since reverse bias current in a pn junction can be considered negligible (and $I_G = 0$), substrate current will also be inconsequential ($I_{sub} = 0$).Thus only the drain current I_D which flows between the source and drain in the MOSFET needs to be considered. In summary, three independent terminal voltages and one current, I_D is generally associated with the operation of the ideal MOSFET.

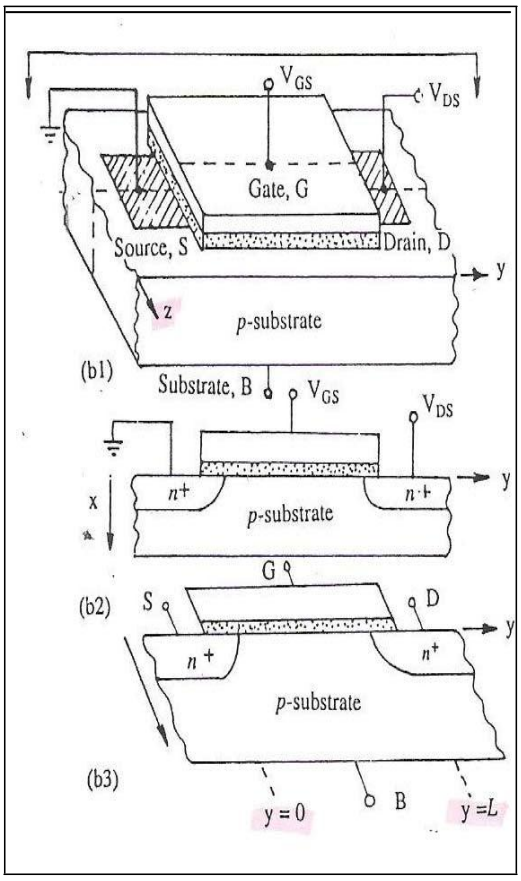


Figure 1.2*: (b1) Perspective view of the MOSFET structure, (b2) Cross section of the MOSFET cut down the middle of the channel, (b3) Cross section of the MOSFET lying flat[11]*

Figure 1.2 defines the axes to be used in the MOSFET structures. That is, the x-direction is perpendicular to the Si-SiO_2 interface (vertical direction), with x = 0 at the Si surface. The y-direction is parallel to the Si surface in the direction from source to drain (lateral or longitudinal direction).Since the source and drain are separated by a distance L or the channel length, y = 0 at the source end of the channel and y = L at the drain end. The z- direction is the other direction parallel to the Si surface (perpendicular to the y-direction) and defines the channel width.

1.2 MOSFET Device Structure

1.2.1 Basics Operation

The operation of a MOS transistor involves the application of an input voltage to the gate electrode. This establishes an electric field perpendicular to the Si-SiO_2 interface in the channel region of the device. The conductance of the channel region can be modulated by varying this electric field. Since an electric field is responsible for controlling the output current flow, such devices are termed field-effect transistors (FETs).

As Wolfs [12] explaining that, If no gate bias is applied, the circuit path between source and drain consists of two back-to-back pn junctions in series. In this case, if V_{DS} is applied, I_D will consist of only the reverse-bias diode leakage current, which is normally negligible. When positive bias is applied to an NMOS transistor gate, however, electrons will be attracted to the channel region and holes will be repelled. Once the positive gate voltage become strong enough to form an inversion layer, an n-type channel is formed that connects the source and drain regions.

According to Ren-Ji theory [13], a drain current, I_D can then flow if a voltage

V_{DS} is applied between the sources and drain terminals. In the simplest analysis, the voltage-induced n-type channel is assumed that it does not form unless the voltage applied to the gate exceeds the threshold voltage, V_T.

As Hess [14] points out MOS devices in which no conducting channel exists when V_{GS} =0, are referred to as enhancement-mode or normally OFF transistors in **Figure 1.3** and **Figure 1.4**.With NMOS enhancement-mode transistors, a positive gate voltage, V_{GS} greater than V_T must be applied to create the channel or to turn them ON, while to turn on PMOS enhancement-mode devices, a negative gate voltage whose magnitude is $>V_T$, must be applied. Note that in NMOS transistors a positive voltage must also be applied to keep the drain-substrate reversed-biased, while in PMOS devices this voltage must be negative. On the other hand, it also possible to build MOS devices in which a conducting channel region exists when V_{GS} =0V and such MOS devices are described as being normally ON. Since a bias voltage to the gate electrode is needed to deplete the channel region of majority carriers, and thus turn them OFF, such devices require a negative gate voltage to be turned OFF, while corresponding PMOS devices require positive gate voltage.

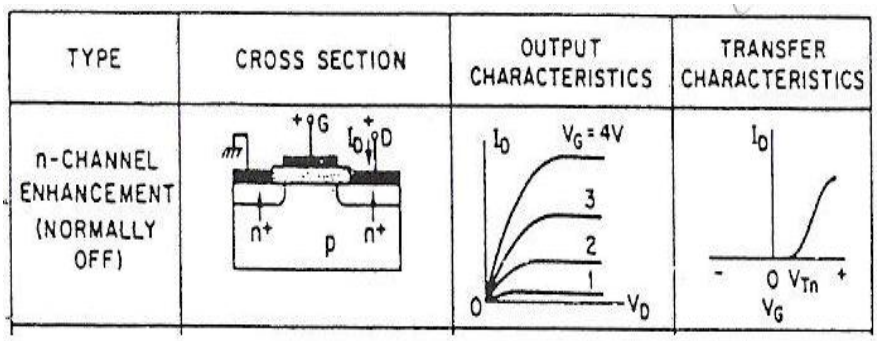


Figure 1.3 : *N-channel enhancement mode [11]*

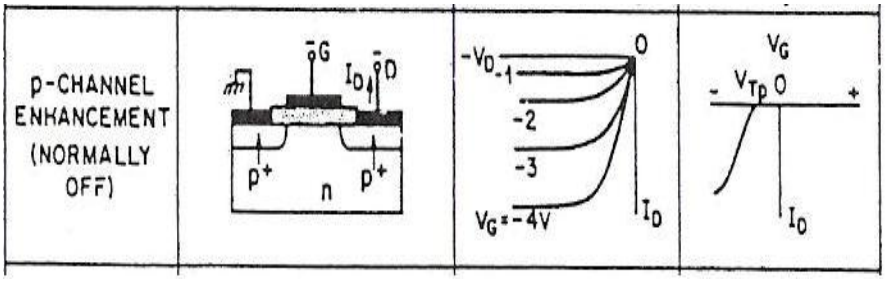


Figure 1.4: *P-channel enhancement mode [11]*

1.2.2 Biasing the Inversion Layer

An external bias voltage can be applied to the channel region of a MOS structure) if an inversion layer has been induced there. It is called "communication". On the other hand, if the channel region is not inverted, the application of a bias voltage to a diffused region adjacent to the channel region will have no effect on the surface potential in the channel. Such "communication" has the following impact on the behavior of a MOSFET.

1. If the gate voltage applied to a MOSFET is less than the threshold voltage, the device said to be operating in the subthreshold regime.
2. If the channel is inverted, and channel–bulk voltage, V_{CB} is increased, the depletion region of the field-induced channel increases. If gate-bulk voltage, V_{GB} is held fixed, the number of electrons in the inversion layer will decrease as V_{CB} is increased. At some value of V_{CB} the inversion layer charge will entirely disappear.
3. "Communication" with the channel also permits the diffused region to become an additional source of mobile carriers to the channel.

1.3 Long Channel MOSFET

1.3.1 Circuit Characteristics

From the perspective of the MOSFET as a circuit component, long-channel behavior has been specified in a number of ways. A list of device parameters from a circuit perspective deemed to be characteristics of long-channel MOSFETs include the following:

1. The threshold voltage V_T is independent of channel length L.
2. The threshold voltage V_T is independent of drain bias voltage, V_{DS}.
3. The drain current in saturation I_{Dsat} is independent of V_{DS}.
4. The drain current has a linear dependence on 1/L.
5. The subthreshold current I_{DSt} is independent of drain bias.
6. The subthershold swing St is independent of gate length.

1.4 Threshold Voltage Control in MOSFETs

Qiang Chen.et al [15] in explaining the definition of the threshold voltage is the value of the gate voltage that turns on the transistor by inducing a highly conductive channel from the source to the drain. While, Michael Shur [16] found that depending on the applied gate to source bias, V_{GS}, any field effect transistor can be either in the on-state with a conducting channel between the source and drain, or in the off state, with practically no conduction between the source and drain. The gate voltage, V_T separating these two regimes is called the threshold voltage.

The factors that impact V_T is given in Equation (1).An examination of each term will reveal the device parameters that can be adjusted to provide practical control of V_T.

$$V_T = \varphi_{ms} - Q_{ot}/C_{ox} + 2\sqrt{\kappa_{si}\varepsilon_o q N_{sub}\varphi_B}/C_{ox} + 2\varphi_B \quad \text{.....(1)}$$

The φ_{ms} term depends on work function difference between the gate, $q\varphi_m$ (gate), and the semiconductor, $q\varphi_B$ (sub).While $q\varphi_m$ (gate) for metal and heavily doped silicon gates is constant, the parameter Φ_B (sub) depends on the substrate doping- but only in a logarithmic manner. Hence, each factor of 10 increase in substrate doping will change the φ_{ms} term by only 2.3Kt/q or ~0.06 V (kT / q =0.026V at 300K).Thus, changes in the substrate doping concentration produce changes in V_T through the φ_{ms} term); thus, the $2\varphi_B$ term is also ineffective for controlling V_T. Since every attempt is made to keep Q_{tot} as low s possible through various processing procedures and C_{ox} is relatively large (since t_{ox} is very thin in submicron MOSFETs), the Q_{tot}/C_{ox} term is also very small in modern MOSFETs. Hence, this term must also be ruled out as a candidate for controlling V_T. While is true that C_{ox} could be varied (primarily by changing t_{ox}), this is not a practical approach to controlling V_T in active devices, since tox is normally made as thin as possible to maximize I_D. This leaves $2\sqrt{\kappa_{si}\varepsilon_o q N_{sub}\varphi_B}/C_{ox}$ term as the remaining candidate for controlling V_T in active devices. Since the change of V_T in this term depends on $\sqrt{N_{sub}}$, it indicates that V_T control is possible by exploiting this effect.

Merely increasing the substrate doping, however, is not desirable since it will adversely impact other MOSFET characteristics, such as lower junction- breakdown voltages, larger junction capacitance, and lower carrier mobility. Yet, prior to the development of ion implantation in the early 1970s, adjustment of substrate doping was the only practical processing approach for significantly controlling V_T in active devices.

1.4.1 Ion Implantation for Adjusting Threshold Voltage

Implantation can be used either to increase or to decrease the net dopant concentration at the silicon surface. As a result, substrate doping can be selected strictly on the basis of optimum device performance since V_T can now be set by the V_T adjust implant process. In addition, since dopants can be selectively implanted into the field regions, high performance NMOS circuits can be fabricated on lightly doped substrates, without the possibility of inadvertent inversion of the surroundings field regions.

As mentioned earlier, the V_T adjust implant technique involves implantation of boron, phosphorus, or arsenic ions into the regions under the gate oxide of MOSFET. Boron implantation produces a positive shift in V_T, while phosphorus or arsenic implantation causes a negative shift. For shallow implants, the procedure has essentially the same effect as placing an additional sheet of "fixed" charge at the SiO_2-Si interface.

1.5 Subthreshold Currents in Long Channel MOSFETs

The small drain current which flows in the MOSFET channel below threshold (in weak inversion) is called subthreshold current, I_{Dst}. In most application I_{Dst} is far too small to be useful as a drive current. However, it can represent an unwanted leakage current, especially in ICs designed for low power applications. The common range of V_T in submicron digital CMOS ICs is 0.6V – 0.8V.Thus, when V_{GS} = 0V the MOSFETs in these circuit may be close to weak inversion.

Consequently, for many applications, subthreshold leakage must be well characterized so that the total IC leakage current of the chip can be predicted during the design phase of the product. It should also be noted that the V_T-adjust implant generally increases the subthreshold swing St, and this is one reason that St in real devices is larger (~100Mv/dec) than the theoretically predicted value of ~60Mv/dec at 300K.

1.5.1 Subthreshold Swing, St

The subthreshold swing, St is the gate voltage change that is required for an order-of-magnitude change of the drain current in the subthreshold region. The St of a short channel is impaired by the source or drain. In the subthreshold region, the gate voltage is applied to keep the electrostatic potential of the channel sufficiently low to reduce the amount of mobile carriers in the channel and turn off the transistor. As the channel length is made sufficiently large, the subthreshold swing approaches its ideal value given by [17], i.e.,~60mV/dec at room temperature. As the channel length (L) of a typical MOSFET is reduced with all other parameters held constant, the threshold voltage decreases and the subthreshold swing, St increases. Since L decreases, the lateral fields terminate on more charge further into the channel, which essentially steals the charge that would normally be terminated by the gate voltage in a along channel devices. This stealing of charge by the lateral fields effectively lowers the source-to-channel barrier, which controls the conduction of electrons from source to drain. As P. Vandamme et. al [18] in explaining that St depends on gate source voltage, V_{GS} and has minimum value at V_{GS} which is linearly related to the voltage at which moderate inversion starts.

For large V_{GS} the drain current starts to deviate from its exponential behaviour and St is increase. According to threshold voltage roll-off and subthreshold swing rollup are commonly known as short channel effects (SCEs).In MOSFETs with uniformly doped substrates, St is calculated from

$$St = \ln 10 \, (d\ln I_D / dV_{GS})^{-1} = 2.3 \, (kT/q) \, (1+Cd/Cox) \quad (2)$$

$$= 2.3 \, (kT/q) \, [1+\kappa_{si} t_{ox}/\kappa_{ox} d)] \quad (3)$$

The factor 2.3 comes from the conversion of ln(x) to $2.3\log_{10}[x]$.

Ideally, an abrupt change in I_D should occur as V_{GS} passes through V_T. If a MOSFET exhibits a steep decline in I_D as V_{GS} is decreased below V_T, its St value will be small. Conversely, is a MOSFET structure is known to posses a small St, the implication is that only a small reduction of V_{GS} below V_T will effectively turn off the device; whereas if the device exhibits a large St value, a significantly large I_{DST} may still flow in the OFF state (when $V_{GS} = 0$).

According to equation (3), at 300K in the ideal limit of $t_{OX} = 0$, St = (2.3Kt/q) ~60mV /dec value (also, note that is T increases, so does the value of St).The St value of typical interfaces states, or a nonzero value of tox) cause St to become larger than the 60mV/dec value (also, note that if T increases, so does the value of St). Thus, if St is known, equation (2) can be used to estimate I_{Dst} in long channel MOSFETs in subthreshold operation. That is, circuit designers can readily calculate the gate bias required to keep the subthreshold negligibly small, the maximum bias applied to the gate when the devices is in the OFF state should be kept at least 0.5V below V_T.

Equation (2) also indicates that St can be made smaller by using a thinner tox or a lower substrate doping concentration which will make the channel depletion-region width, d larger. In addition, equation (2) implies that St increases with temperature. Finally, it should be noted that because the depletion width increases when a substrate bias is applied, the subthreshold swing decreases according to equation (3). **Figure 1.5** shows that the impact of short channel effects on drain current. As the channel length (L) is reduced, subthreshold swing increases ($S_2 > S_1$) and threshold voltage decreases ($V_{TH2} < V_{TH1}$) [15]

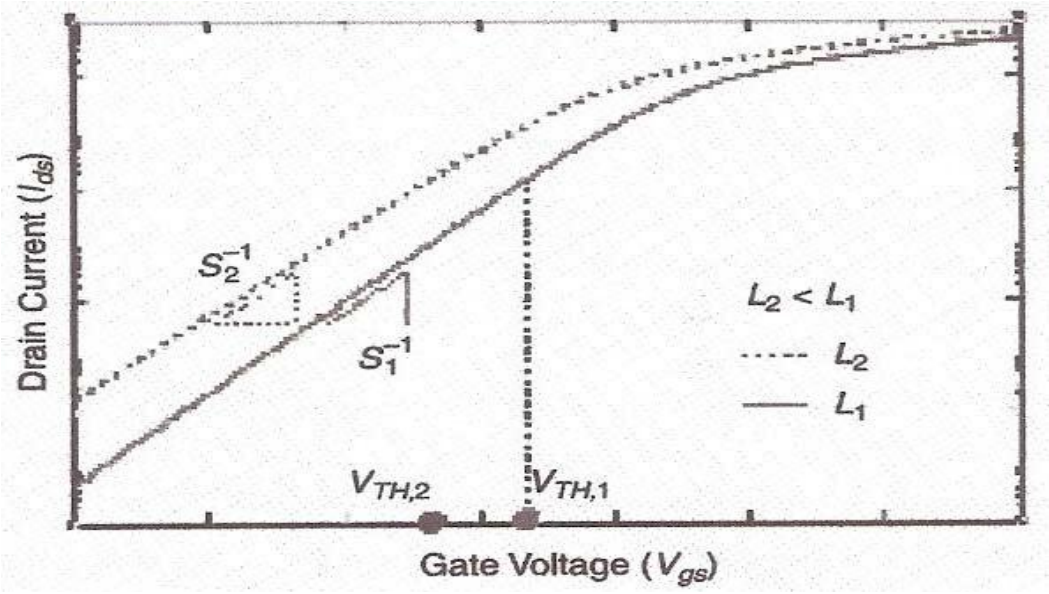


Figure 1.5*: Graph of drain current, I_D vs gate voltage, V_{GS} [15]*

1.5.2 Gate Induced Drain Leakage (GIDL)

Another form of leakage current observed in OFF state MOSFETs is *gate- induced drain leakage* (GIDL).The carriers responsible for GIDL originate in the region of the drain that is overlapped by the gate, and GIDL is occurs when the gate is grounded and the drain is at VDD.A large electric field then exists across the oxide (ε_{OX}), which must be supported by charge in the drain region. This charge is provided by the formation of a depletion region in the drain.

1.6 The submicron MOSFET

Since the quest for higher density still requires L and Z to be further reduced, it will nevertheless be necessary to confront the other short channel effects. Increased "off-state" leakage in short channel MOSFET is due to several phenomena including, lowering of the threshold voltage V_T as L is decreased and/or V_{DS} is increased, the onset of punchthrough at smaller drain biases as L is decreased, and an increase in isolation leakage current as the isolation spacing is decreased. The reliability problems that arise in short MOSFETs include this gate oxide breakdown, device degradation due to hot carrier effects; and reliability problems associated with the interconnects between MOSFETs, such as electromigration failures in the metal lines.

1.6.1 Comparison of Long Channel and Short Channel MOSFET Characteristics

As a result, short channel device effects can be correlated with reduction in the gate length and/or gate width dimension. Long channel device characteristics that undergo variation as the gate dimensions are decreased.

From the comparison above, we can see that the short channel effects can be divided into the following categories: (a) those that impact V_T, (b) those that impact subthreshold currents; and (c) those that impact I_D when the MOSFET is operated in saturation, $V_{DS} > (V_{GS} - V_T)$.

Long Channel MOSFET Behavior

1. The threshold voltage, V_T is independent of channel length L and width Z.
2. V_T is independent of drain bias voltage.
3. V_T depends on V_{BS}
4. The subthreshold current I_{Dsat} increases linearly as L decreases.
5. I_{Dst} is independent of drain bias.
6. The subthreshold swing St is independent of gate length.
7. The drain current in saturation I_{Dsat} is independent of V_{DS}.
8. I_{Dsat} is proportional to $(V_{GS}- V_T)^2$
9. I_{Dsat} is proportional to 1/L

Short Channel MOSFET Behavior

1. V_T decreases as L is decreased. V_T may also be impacted by changes in Z.
2. V_T decreases with increasingly V_{DS}
3. V_T increases less rapidly with V_{BS}
4. I_{Dst} increases more rapidly than linearly as L is decreases
5. I_{Dst} increases with increasing V_{DS}
6. St increases with decreasing L
7. I_{Dsat} increases as V_{DS} increases
8. I_{Dsat} is proportional to $(V_{GS} - V_T)$
9. As $L \rightarrow 0$, I_{Dsat} becomes independent of L

1.7 Punchthrough in Short Channel MOSFETS

Punchthrough is a phenomenon associated with the merging of the source and drain depletion regions in the MOSFET. That is, as the channel gets shorter, these depletion region edges get closer. When the channel length is decreased to roughly the sum of the two junction depletion widths, punchthrough is established. Nevertheless, since the depletion regions of a pn junction widen as reverse bias is increased, all MOSFETs would eventually enter punchthrough if a high enough V_{DS} could be applied. However, in MOSFETs with L>2.0μm, breakdown of the drain substrate junction generally sets in before this punchthrough voltage is reached. As a result, in practice, punchthrough is not a limiting factor in long channel digital MOSFET design. In shorter channel device, however, punchthrough does represent a serious limitation.

1.8 Short Channel Effects on the I-V Characteristics of MOSFETS Operated in the Strong Inversion Regime

Short channel effects significantly alter the dc I_D-V_{DS} characteristics of long channel MOSFETs being operated in strong inversion in three ways. First, the combined effects of reduced gate length and gate width produce a change in V_T. Second, the mobility of the carriers in the channel is reduced by two effects, which in turn reduces I_D. These two effects are the mobility degradation factor (due to the gate length), and the velocity saturation factor (due to the lateral channel field).Third, the channel length is modulated by the drain voltage when the devices is in saturation, when $V_{DS} > (V_{GS} - V_T)$, causing an increase in I_{Dsat} with increasing V_{DS} (channel modulation effect).

1.9 MOSFET Scaling and challenges:

Over the past decades, the improvement in performance of complementary metal–oxide–semiconductor (CMOS) technology has been extremely rapid and it is the backbone of the incredible advancements in digital technology. One of the main driving forces behind the improvement is downscaling of the metal-oxide-semiconductor field-effect transistor (MOSFET). Over the past 50 years, the number of transistors has doubled every two years.
This trend, first observed by Gordon Moore [1], is very interesting; especially that it has been possible to continue this exponential growth for such a long time. The rate of growth is related to the economics of scaling. Though scaling makes fabrication of each transistor cheaper, development of a new technology is, nonetheless, expensive. The rate of development does not have to be limited by Moore's law, but since the law has held for decades, it appears it is difficult for the semiconductor industry to improve faster while remaining profitable.

Generally, by reducing the device dimensions, the density of MOSFETs on the chip is increased, power consumption per device is decreased, and the switching speed can be increased. However, in recent years the scaling has become increasingly challenging, as both limits to existing fabrication technologies and fundamental physical limits, have required many changes in the way the devices are fabricated.

As the gate length (L) is scaled, the source/drain (S/D) junction depth (xj), depletion width (Wd), and oxide thickness (tox) have to be scaled as well, so that the gate maintains electrostatic control over the device. Reduction of tox is limited by leakage tunneling current, which has caused the industry to change to high-k oxides [2]. Reducing Wd requires higher bulk doping which reduces mobility.

In order to circumvent these scaling limitations, fully depleted (FD) structures with a thin Si body, such as ultra-thin-body (UTB), multiple-gate (doublegate, tri-gate, and gate all around) MOSFETs and grooved channel MOSFET's have, in recent years, been the subject of intensive research [3-5].

An innovative approach is needed to allow future reduction of channel length. The multi-gate structure and Recessed Channel MOSFETs are promising candidates [4].

Recessed Channel MOSFET is one such promising candidate because of its quasi planar structure, excellent roll-off characteristics, drive current and it is close to the conventional MOSFET in terms of layout and fabrication as it can be built using standard bulk planar CMOS process[5,6]. Because of better gate control in RC-MOSFET, the Short-channel effects are reduced as compared to a bulk MOSFET [7]. These devices have sharper sub threshold slopes which allow better switching in the device. RC-MOSFET can be used for both analog as well as digital applications. These are considered to be the best candidates for scaling of MOSFETs below 50 nm. [8].

A roadmap of the scaling of MOSFET devices was proposed by Hu in 1993 [19].He assumed that a new generation of technology will continue to be developed every three years, with perhaps a slow-down to four years beyond the 0.35µm generation. His proposal for MOSFET scaling is outlined as follows:

1. The IC industry/market will agree on the next power-supply voltage standard V_{CC} several years in advance of introducing a technology/ product using that voltage.
2. For a given V_{CC}, the thinnest gate oxide will be used to get maximum I_D
3. Junction depths will be scaled aggressively to keep the short channel effects within a desired limit.
4. V_T of general purpose technology will remain basically unchanged. A significant reduction in V_T is unacceptable for channel subthreshold leakage.
5. The well doping concentration or punchthrough implant dose will be increased, and the gate length may be chosen to be larger than the minimum feature size in order to achieve acceptable leakage and standby current.
6. Drain engineered structured will be used as necessary to meet the constraints of hot carrier reliability, breakdown voltage and GIDL.

The fundamental issue of downsizing MOSFETs is to preserve long-channel characteristics after miniaturization. Several approaches have been proposed as roadmaps for designing submicron MOSFETs (L <1μm) so that they exhibit such behavior. Three of the most important scaling methodologies are the constant electric field scaling and its derivatives (constant voltage and constant electrostatics scaling). The method of constant electric field scaling for designing submicron MOSFETs was proposed by Hayes [20].In this approach, a successful larger device structure is selected and all its dimensions and voltages are reduced by a constant scaling factor λ (>1).Then, scaling based on subthreshold behavior, scaling to achieve a desired value of subthreshold current, I_{off}. Because subthreshold conduction is the dominant short channel performance issue that limits MOSFETs scaling.

1.9.1 Subthreshold Swing, St

Another approach to scaling which overcomes the above difficulty was proposed by Brews et al [20].They introduced an empirical formula which determines the minimum gate length a MOSFET can have so that its subthreshold behavior remains insensitive to drain bias. That is, by using this formula a constraint upon each single combination of device parameters is identified, such that if this constraint long channel subthreshold behavior. When long channel devices are operated in subthreshold, I_{Dst} is independent of drain to source voltage once V_{DS} exceeds a few kT/q [20].Thus, the criterion selected to represent acceptable long channel behavior was not more than a 10% change in drain current could occur for a 0.5V change in V_{DS}.

1.9.2 Subthreshold Scaling

When long channel devices are operated in subthreshold, I_{Dst} is independent of drain to source voltage once V_{DS} exceeds a few kT/q. Thus, the criterion selected to represent acceptable long channel behavior was that no more than a 10% change in drain current could occur for a 0.5V change in V_{DS}.

Chapter 2

SIMULATION TOOL AND RESEARCH OBJECTIVE

2.1 Introduction to Device Simulator

ATLAS is a physically-based device simulator. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, onto this grid you can simulate the transport of carriers through a structure. This means that the electrical performance of a device can be modeled in DC, AC or transient modes of operation.

There are three physically-based simulation. These are:

• It is predictive.

• It provides insight.

• It conveniently captures and visualizes theoretical knowledge.

Physically-based simulation is different from empirical modeling. The goal of empirical modeling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity. Empirical models provide efficient approximation and interpolation. They do not provide insight, or predictive capabilities, or encapsulation of theoretical knowledge.

Physically-based simulation has become very important for two reasons. One, it is almost always much quicker and cheaper than performing experiments. Two, it provides information that is difficult or impossible to measure.

Those who use physically-based device simulation tools must specify the problem to be simulated. In ATLAS, specify device simulation problems by defining:

• The physical structure to be simulated.

• The physical models to be used.

• The bias conditions for which electrical characteristics are to be simulated.

2.2 Silvaco ATLAS and DEVEDIT

In my project and thesis work DevEdit 3D version 2.6.0.R and Silvaco Atlas version 5.16.3.R are used to perform RC-MOSFET device simulation and adder implementation using MIXEDMODE simulation.

DevEdit is a device structure editor. It can be used to generate a new mesh on an existing structure or can be used to create or modify a device. DevEdit can be used as a simulator under DeckBuild or through a Graphical User Interface (GUI). DevEdit allows structures to be created or read into DevEdit in the form of SILVACO Standard Structure Files. ATLAS is a physically-based two and three dimensional device simulator. It predicts the electrical behaviour of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation [9].

The DeckBuild run-time environment is used in our project work. The DeckBuild run-time environment receives the input files. Within the input files, Silvaco Atlas is called to execute the code. and finally, TonyPlot is used to view the output or results of the simulation like characteristics plot etc.

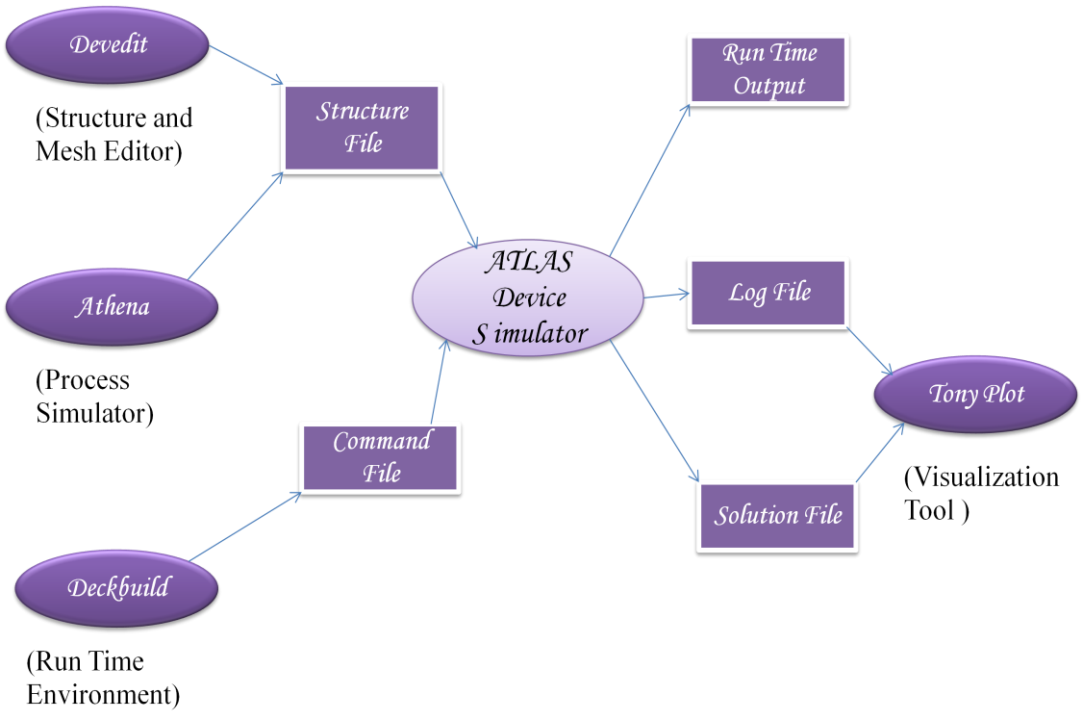


Figure 2.1 *Data flow in ATLAS [9]*

2.3 Research Objective & Outline

The goal of this work is to investigate, through device simulations and a literature study, various device characteristics by varying various device parameters of the RC-MOSFET. The main advantage of the RC-MOSFET is that the leakage current and SCE are under control. There is also increase in the drain current.

So RC-MOSFET is much better than conventional MOSFET. Because of better position of RC-MOSFET the analysis is done in this work that how threshold voltage, leakage current and drive current are affected by varying various parameters of RC-MOSFET and it's logical implementation into Half Adder is analyzed using ATLAS MixedMode Simulation.

This thesis is outlined as follows:-

Chapter 3 Introduction of RC-MOSFET and various structures of recessed channel MOSFET, its working, why it is better and focuses on device simulation details and the literature survey on various results of simulations carried out by altering various parameters of RC-MOSFET like oxide thickness, and different oxide materials.

Chapter 4 Focuses on device simulation details and the various results for Half Adder implementation of Recessed Channel MOSFET using MixedMode Simulation.

Chapter 5 Finally conclusion and future work are drawn.

Chapter 3

RECESSED CHANNEL MOSFET

The search for higher performance of ICs has led to the scaling of MOSFETs down to sub-50 nm and below. The hot-carrier deterioration becomes a stringent limitation to the reliability of sub-50-nm devices and VLSI packing density. Technologists use the hot-carrier-reliability and linearity distortion issues from the device design perspectives. Hot carrier reliability of MOS devices has been studied as a major reliability concern [21]–[25] for the past several decades since the deeply scaled MOS device design suffers from a hot carrier effect and also degrades analog circuit requirements.

As devices are scaled, the benefits of higher electric fields saturate while the associated reliability problems get worse [26]. The presence of large electric fields in MOSFETs implies the presence of high energy carriers or the hot carriers, in such devices, that might get injected into the surrounding dielectric films such as the gate and sidewall oxides [27]. The presence of mobile carriers in the oxides triggers various undesirable physical processes that drastically change the device characteristics during normal operation over prolonged periods of time eventually causing the circuit malfunctioning. The deteriorating effect of gate leakage current and substrate current on the digital and analog device performance has also been discussed recently [28], [29].

It is thus increasingly important to analyze hot carrier reliability in terms of hot-electron-injected gate current, impact-ionization substrate current, and electron velocity and temperature near the drain end for their impact on the overall chip performance, and not just for their impact on device speed, because chip-level power constraints as well as device and process variability and reliability can seriously diminish the value of device

innovations. Furthermore, linearity has been an important figure of merit (FOM) in all RF and wireless applications to guarantee minimum signal distortion in modern communication systems. With the drastic increase in the demands for mobile communication and wireless systems, linear and low-noise system designs have become potential solutions to achieve high-quality system performance for system-on-chip (SoC) designs. Linearity and inter modulation distortion analysis and simulation are thus needed to realize the linearity limiting factors for a given technology as well as to optimize transistor structure and device topology for improved performance.

As the MOSFET dimensions scale down to sub-50-nm regime, further scaling down of SiO_2 gate dielectric leads to high direct tunneling gate leakage current, which, in turn, causes the increase in device power consumption. This critical issue necessitates the introduction of high-*k* materials for sub-50-nm technology node so that the physical thickness of oxide layer ($t_{ox} = t_{ox1} + t_{ox2}$) increases, keeping the effective oxide thickness (EOT) same [38]–[41]. The CMOS transistors designed with multilayer high-*k* gate dielectrics achieve the expected high drive current performance and lower leakage current, thereby proving its efficacy for high-performance CMOS logic applications. The metal gate/high-*k* dielectric and SiO_2 multilayered gate architecture exhibit negligible gate oxide leakage and channel mobilities close to SiO_2 [38], [41].

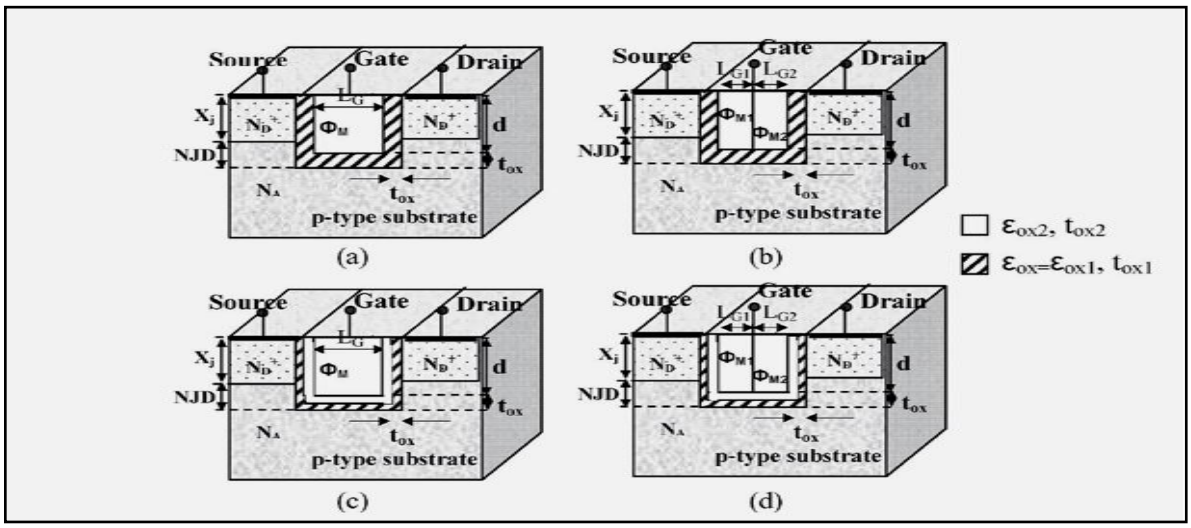


Fig.3.1 *Schematic cross-sectional view of (a) RC, (b) GEWE-RC, (c) MLaG-RC, and (d) MLGEWE-RC MOSFET designs.*

3.1 RECESSED CHANNEL MOSFET DESIGNS:
GATE ELECTRODE WORK FUNCTION AND GATE DIELECTRIC ENGINEERING

Ever advancing innovative techniques and novel architectures involving various channel engineered structures, such as recessed channel (RC) [Fig. 3.1(a)] [42]–[45] and gate electrode Work function engineered (GEWE) structures [46]–[49], are now given extensive consideration. RC MOSFET is considered as a capable candidate for suppressing short channel effects (SCEs) and improving the hot-carrier immunity and, thus, the device reliability [50]–[54].

In the RC MOSFETs, since the drain and source regions are separated from one another through a groove, the extension of the drain electric field toward the channel region is restrained. Thus, the presence of groove minimizes the SCEs and punch through effects, thereby enhancing the hot-carrier reliability. In this structure, two potential barriers are formed at the corners, referred to as the "corner effect," due to the high density of electric field lines at the corners, which leads to SCE immunity. Furthermore, as the negative junction depth (NJD) increases (or the source/drain junction depth decreases), the potential barriers augment. The carrier velocity thus goes down, causing the drain current driving capability to degrade. Moreover, the charge carriers now require high energy to surmount the potential barriers, thereby raising the device's threshold voltage.

RC MOSFET, however, in conjunction with the structure incorporating gate electrode work function engineering such as dual-material-gate (DMG) architecture, as shown in Fig. 3.1(b), enhances drain current characteristics and average carrier velocity and suppresses SCEs due to the screening of the channel region from drain bias variations [47], [48]. Furthermore, to counteract the large gate leakage and increased standby power consumption that arises due to continued scaling of SiO_2-based gate dielectrics, the multilayered gate oxide architectures have also been accounted for in our study as shown in Fig. 3.1(c) and (d). High-k gate dielectric becomes a key in providing the increased physical gate dielectric thickness t_{ox} (= t_{ox1} + t_{ox2}), keeping the EOT (t_{oxeff}) same, without

compromising the direct tunneling gate leakage current. Increasing the physical gate dielectric thickness, however, results in a higher gate-fringing field, thereby reducing the gate control and, hence, aggravating the SCEs [39]–[41]. Fig. 3.1(c) corresponds to the multilayered gate RC (MLaG-RC) MOSFET, and Fig. 3.1(d) corresponds to the multilayered GEWE RC (MLGEWE-RC) MOSFET.

With GEWE-RC MOSFET structure, there is considerable improvement in the hot-carrier reliability, owing to perceivable step in the surface potential profile that screens the control gate from drain potential variations. The focus is on the exploration of various important aspects of GEWE-RC and its gate stack architecture counterpart for improving the hot-carrier immunity of scaled devices such as conduction band offset, gate leakage current due to hot-electron injection at the drain end, substrate current due to impact ionization, electron velocity, and electron temperature for providing reasonable bounds in the design and parametric optimization. We can assess both GEWE-RC and conventional RC MOSFETs in addition to bulk; the role of multilayered gate architecture, in terms of device analog and large signal performance; and the impact of gate stack architecture and other structural design parameters such as gate length, NJD, NA, V_{SUB}, V_{DS}, ε_{ox2}, and metal gate work function variation on the device evaluation metrics.

3.2 DEVICE FABRICATION FEASIBILITY

In order to improve and enhance the life span of conventionally scaled MOSFET designs, various designs are approaching the device realization scenario. The work thus supplements this precondition by proposing and investigating the hot-carrier reliability, linearity inter modulation issues, and analog device performance of GEWE-RC MOSFET employing various engineering schemes, namely, lateral channel engineering by using RC and gate electrode work function engineering by using DMG architecture. In addition to this, study has also been carried out to investigate the impact of gate stack architecture on the device performance of GEWE-RC-MOSFET.

From the simulation study using ATLAS (Chapter 4) device simulator [56], it has been shown that the upshot of these engineering combinations can boost the hot-carrier reliability, and the linearity-inter modulation issues and analog device performance of conventional devices.

For the feasibility of RC MOSFET structure, several integration schemes have been suggested such as plasma etching and LOCOS isolation [43], reactive ion etching and LOCOS isolation technique [44], self-aligned chemical–mechanical polishing (CMP) where the self-aligned process was defined by the groove etching and polysilicon CMP steps [57], and shallow trench isolation where gate oxide films were produced with a conventional furnace and the oxide films for gate electrode were deposited by LP-CVD at 850 ◦C [58]. For the feasibility of DMG architecture, the various available integration schemes are tilt angle evaporation metal gate deposition [42], metal inter diffusion process [59], [60], CMP [61], and fully silicided metal gate [62]. To add further, in 2006, Na and Kim [63] have successfully fabricated DMG architecture by poly-Si gate doping control of the source and drain side gate individually.

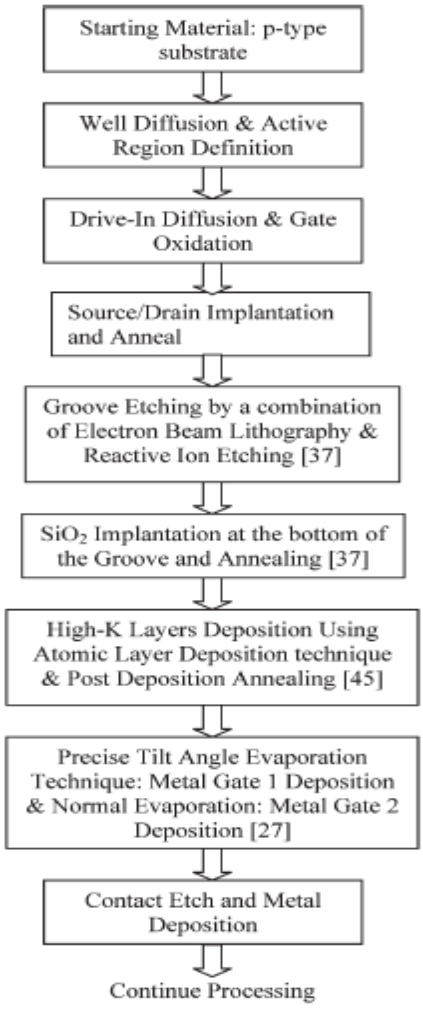
Moreover, in addition to this, fabrication schemes are also available for high-*k* gate stack architectures such as reactive sputtering and oxidation [60], atomic layer deposition technique [64], and plasma nitridation coupled with metal-organic chemical vapor deposition [65].

The MLGEWE-RCMOSFET [Fig. 3.1(d)] is thus proposed with optimistic outlook. The technical manufacturing feasibility of MLGEWE-RC MOSFET is not far reaching in the light of various integration schemes discussed earlier. As mentioned by Xiao-Hua *et al.* [37], by adopting the reactive ion etching and electron beam lithography techniques, the RC architecture implementation into the MOS devices still provides excellent short-channel and hot-carrier-effect immunities. The fabrication process flow for the RC structure is compatible with most of the existing CMOS processes.

Thus, the performance enhancements such as SCE suppression and hot-carrier-effect immunity obtained from the RC structure can be easily achieved using a process flow that is not much more complicated than that used for fabricating the conventional planar devices. Moreover, a double-recessed heterostructure FET has also been fabricated recently so, fabricating a single-recessed structure should not pose any difficulty. A proposed summary of the process flow, outlining the fabrication process of MLGEWE-RC MOSFET and its integration with the standard CMOS process, is shown in Table 3.1.

TABLE 3.1

SUMMARY OF THE STANDARD CMOS PROCESS FLOW WITH MLGEWE-RC IMPLEMENTATION



3.3 Comparison with BULK MOSFET and advantages:

In comparison with BULK MOSFET RC MOSFET is better in terms of improved drain current, drain-induced barrier lowering (DIBL), threshold voltage, intrinsic gain, device efficiency, and early voltage for low power low-voltage analog circuit applications, and switching characteristics in terms of I_{ON}/I_{OFF}, sub threshold slope, and high-speed digital and switching applications.

There is reduction in hot-electron-injected gate current, electron velocity and electron temperature near the drain end, and impact-ionization substrate current is achieved with GEWE-RC MOSFET, thereby enhancing the hot-carrier reliability of the device. Using higher metal work function difference and ε_{ox2}, along with lower NJD, tremendously enhances the short-channel immunity offered by GEWE-RC MOSFET, owing to greater gate controllability over the channel. GEWE-RC MOSFET hot-carrier immunity can further be improved by careful tuning of the device parameters such as Φ_{M2}, ε_{ox2}, NJD, and L_G. Thus a GEWE-RC MOSFET design as a promising solution for realizing CMOS technology for high-performance applications where device reliability is a major concern.

With MLaG-RC and MLGEWE-RC, due to improved gate controllability over the channel, DIBL is significantly lowered, resulting in $\_\Psi_{MLaG}$ = 32 mV and $\_\Psi_{MLGEWE}$ = 19 mV.
This is reflected that in Fig. 3.2 where the DIBL effect is reduced with gate stack architectures. Moreover, with the increase in the applied drain to source bias, the DIBL effect increases, but this increase is significant in bulk and RC MOSFETs in comparison to the proposed designs, mainly due to improved gate control in the latter.

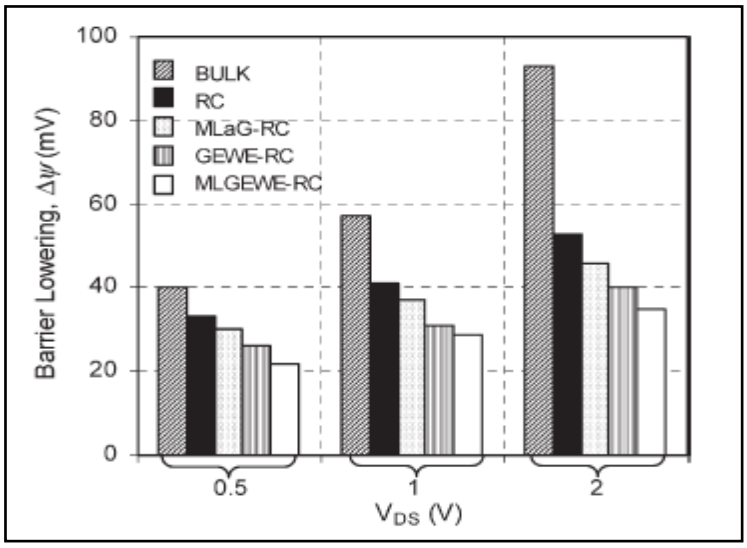


Fig. 3.2 *DIBL versus V_{DS} variation for all RC device designs. Barrier lowering is evaluated with reference to V_{DS} = 0.1 V [49].*

Moreover, as shown in Fig. 3.3 the impact ionization substrate current becomes more important as the drain bias is increased due to the increase of the electric field and current density near the drain region.

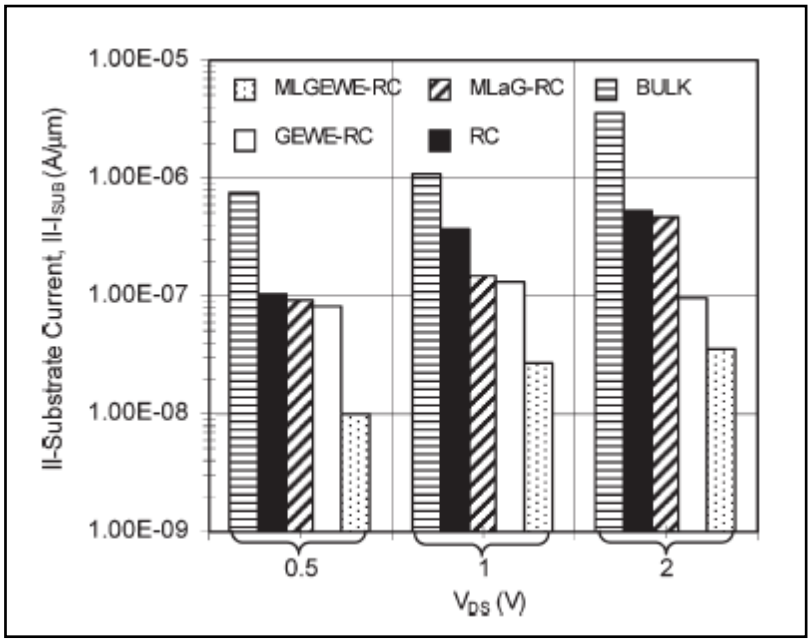


Fig. 3.3. *Impact-ionization substrate current versus VDS for all RC device designs for $V_{GS} - V_{TH}$ = 0.3 V [55].*

MLGEWE-RC MOSFET exhibits the lowest impact-ionization substrate current in contrast to the conventional bulk MOSFET proving its superior hot-carrier efficiency. For low-power and low-voltage analog circuit applications, low II-I_{SUB}, HE-I_G, and lower electron velocity and temperature near the drain end are important design parameters. With proper choice of various structural parameters like εox2, Φ_{M2}, and NJD, II-I_{SUB} and HE-I_G can be appreciably lowered.

Chapter 4

Half Adder Circuit Implementation based on RC-MOSFET using MIXEDMODE Simulation

Arithmetic operations are widely used in many VLSI applications. Addition is a very basic operation in arithmetic. A Half adder based on NMOS inverter is introduced which only uses inverters and transmission gates. This Half adder has a simple structure but it operates very well and results in remarkable advances in reducing power in comparison to other well-known designs. This reduction is due to simple structure, reduced number of transistors and the lowering in switching activities. Again, it is worth mentioning that in the proposed design only a few inverters and pass gates have been used, thus the number of transistors have been decreased. The 1-bit Full Adder cell is the building block of an arithmetic unit of a system and full adder can be further implemented using Half adder Thus, its performance directly affects the performance of the whole system. In other words, increasing the performance of a 1-bit Full Adder cell is very critical for increasing the overall performance of the system.

Addition is a very basic operation in arithmetic. Subtraction, multiplication, division and address calculation are some of the well-known operations based on addition. These operations are widely used in many VLSI applications, since the full-adder cell is the building block of the binary adder, enhancing the performance of the 1-bit full-adder is a significant goal and has attracted much attention. Two important attributes of all digital circuits are reducing power consumption and increasing speed. Full Adder and Half Adder can be comprised of inverters, Universal gates such as NOR, NAND and MAJORITY-NOT gates or can be implemented with a set of inverters.

To implement NAND Gate it is just enough to use high-V_{th} NMOS and low-V_{th} PMOS. For implementing NOR gate, high-V_{th} PMOS and low-$_{Vth}$ NMOS have been used and finally in

order to have MAJORITY-NOT Function both transistors are replaced with high-V_{th} transistors.

The circuit for implementing the universal gates is illustrated in Fig. 4.1 & Fig. 4.2. Because of just two transistors the supply voltage can be reduced .In this situation Pshort-circuit is eliminated and because of low voltage scaling, Pdynamic is reduced in a quadratic manner. So the average power dissipation is lower than conventional CMOS gates. Although lowering supply voltage and modifying the threshold voltage results in decreasing the power consumption, modifying V_{th} and reducing supply voltage have direct influence on latency of the circuit. To implement NAND Gate with Fig. 4.1 it is just enough to use high-V_{th} NMOS and low-V_{th} PMOS. For implementing NOR gate, high-V_{th} PMOS and low-V_{th} NMOS have been used and finally in order to have MAJORITY-NOT Function both transistors are replaced with high-V_{th} transistors.

Using high-threshold voltage transistors and low-threshold voltage transistors in addition to normal-threshold transistors have been accomplished in low- power application and many circuits have enjoyed this technique in low-power design. Multi-threshold CMOS(MTCMOS)circuits and dual-V_{th} techniques use high-V_{th} transistors to eliminate and reduce the leakage current through a transistor, thereby decreasing leakage power consumption while maintaining performance. So reducing the leakage power and the propagation delay time to design energy efficient high speed circuit with low-power-delay product is achievable by using modified threshold voltage transistor in circuit path .

A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions *low* (0) or *high* (1), represented by different voltage levels. Static logic Gates are NAND, NOR, NOT.

The *NAND gate* operates as an AND gate followed by a NOT gate. A Low output results only if both the inputs to the gate are High. If one or both inputs are Low, a High output

results. NAND gates can also be made with more than two inputs, yielding an output of Low if all of the inputs are High, and an output of High if any of the inputs is Low. These kinds of gates therefore operate as n-ary operators instead of a simple binary operator. The *NOR gate* is a combination OR gate followed by an inverter. A High output (1) results if both the inputs to the gate are Low (0). If one or both input is High (1), a Low output (0) results. NOR is the result of the negation of the OR operator. NOR is a functionally complete operation—combinations of NOR gates can be combined to generate any other logical function. A logical *inverter*, sometimes called a *NOT gate* to differentiate it from other types of electronic inverter devices, has only one input. It reverses the logic state. The CMOS 1-bit full adder cell has 28 transistors. The CMOS structure combines PMOS pull-up and NMOS pull down networks to produce considered outputs

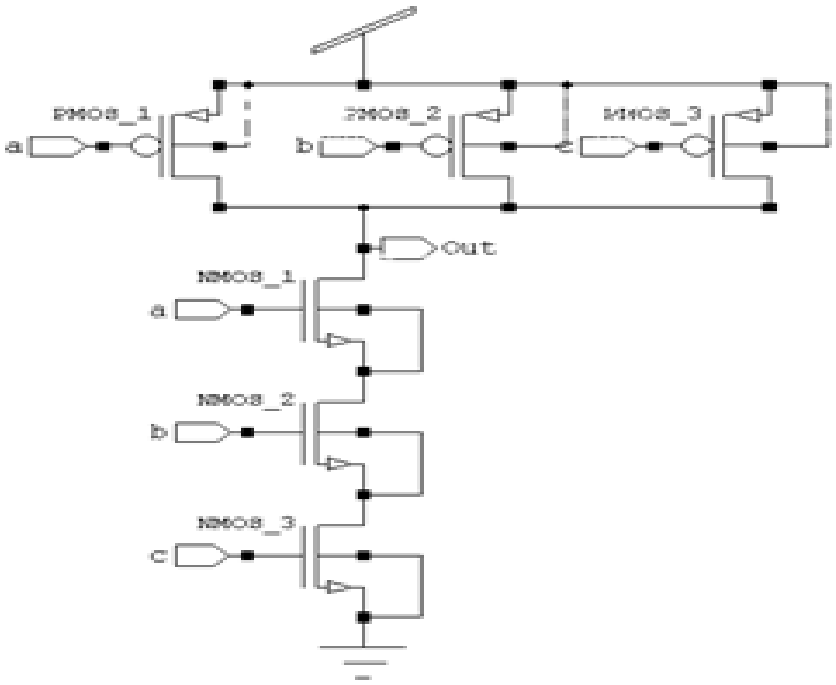


Figure. 4.1 *Conventional NAND Logic Gate*

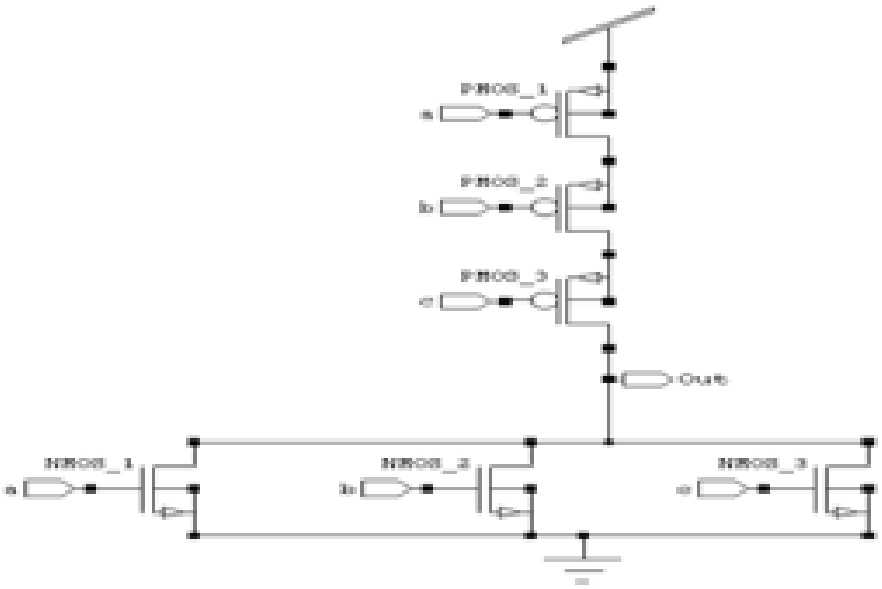


Figure 4.2 Conventional NOR Logic Gate

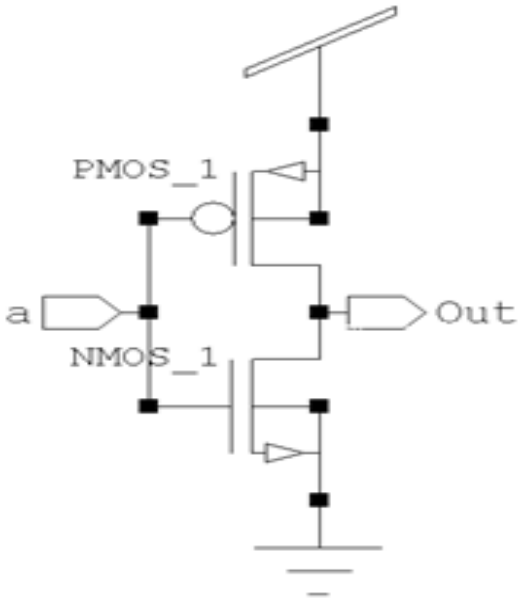


Figure 4.3 Conventional NOT Logic Gate

4.1 Half Adder Design:

An Adder circuit is a combinational digital circuit that is used for adding two numbers. A typical adder circuit produces a sum bit (denoted by S) and a carry bit (denoted by C) as the output. Typically adders are realized for adding binary numbers but they can be also realized for adding other formats like BCD (binary coded decimal), XS-3 etc. Besides addition, adder circuits can be used for a lot of other applications in digital electronics like address decoding, table index calculation etc. Adder circuits are of two types: Half adder ad Full adder.

Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. From this it is clear that a half adder circuit can be easily constructed using one X-OR gate and one AND gate. Half adder is the simplest of all adder circuit, but it has a major disadvantage. The half adder can add only two input bits (A and B) and has nothing to do with the carry if there is any in the input. So if the input to a half adder have a carry, then it will be neglected it and adds only the A and B bits. That means the binary addition process is not complete and that's why it is called a half adder. The truth table, schematic representation and XOR//AND realization of a half adder are shown in the figure 4.4 below.

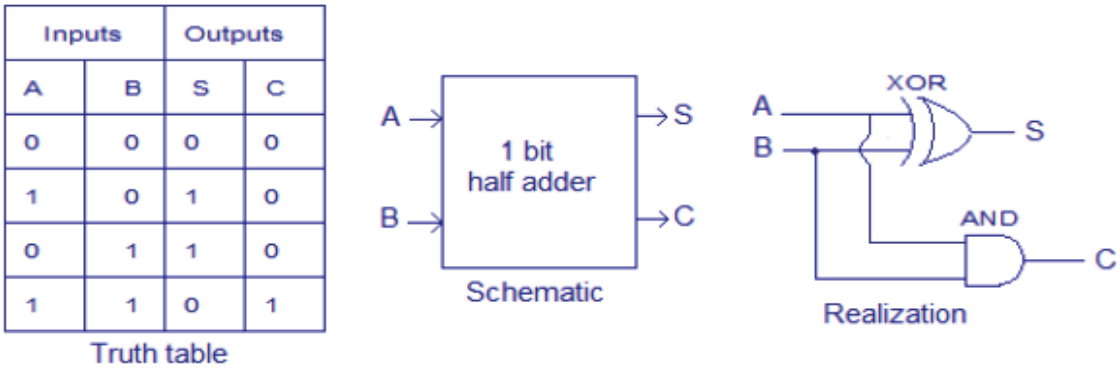


Fig 4.4 *Truth table, schematic and realization of half adder*

NAND gates or NOR gates can be used for realizing the half adder in universal logic and the relevant circuit diagrams are shown in the figure 4.5 below-

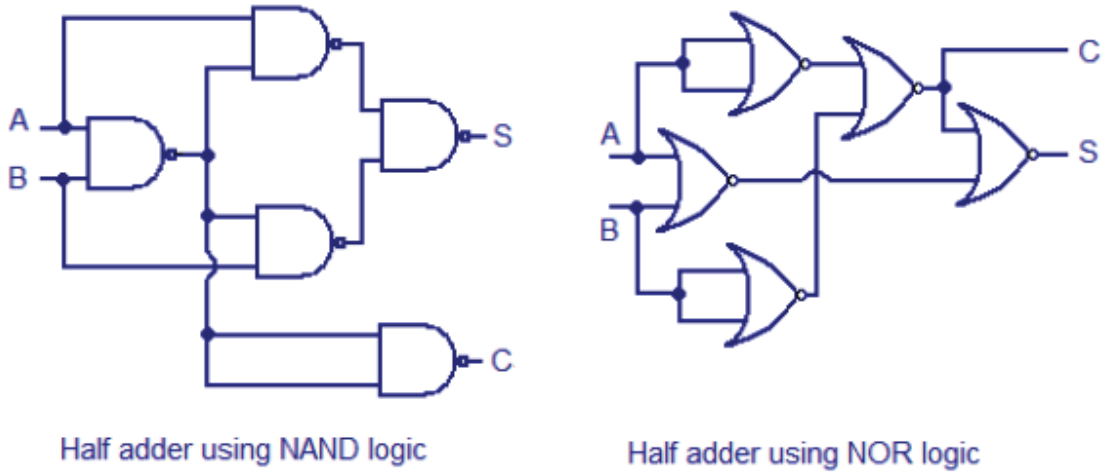


Fig 4.5 *Half adder using NAND & NOR logic gate*

4.2 Half Adder design using NAND gate designed by MIXEDMODE Simulation:

NAND is a universal logic gate and thus Half adder can be implemented using the NAND gate. Here first of all a NAND gate is designed which can further be used as a sub circuit for Half adder circuit design.

Using NMOS technology we are designing a NAND gate in which there are two types of NMOS structures is used-

(a) First one is ATLAS Simulated.

(b) Second is SPICE Simulated.

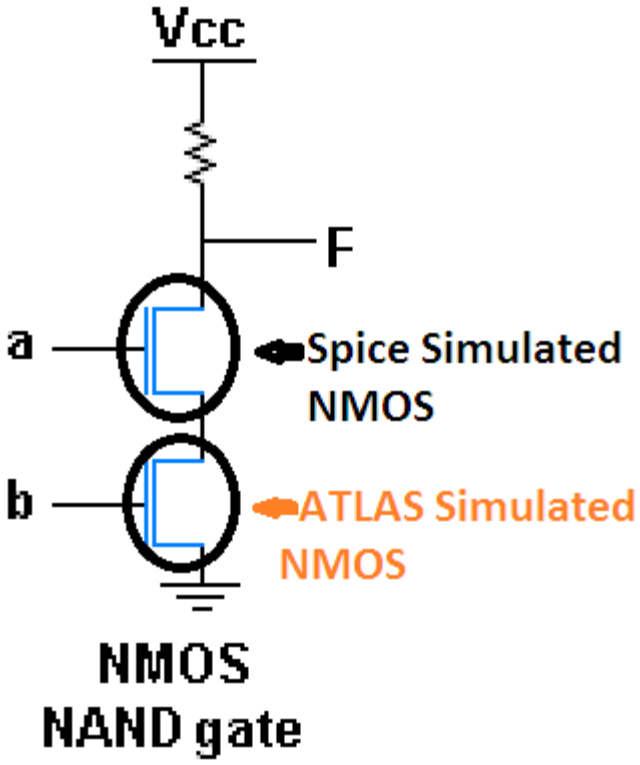


Fig 4.6 *NAND gate designed using MIXEDMODE Simulation*

4.3 MIXEDMODE Simulation:

4.3.1 Overview

MIXEDMODE is a circuit simulator that can include elements simulated using device simulation and compact circuit models. It combines different levels of abstraction to simulate relatively small circuits where compact models for single devices are unavailable or sufficiently accurate. MIXEDMODE also allows you to also do multi-device simulations. MIXEDMODE uses advanced numerical algorithms that are efficient and robust for DC, transient, small signal AC and small signal network analysis.

MIXEDMODE is typically used to simulate circuits that contain semiconductor devices for accurate compact models that don't exist or circuits where devices play a critical role must be modeled accurately. Applications of MIXEDMODE include: power circuits that may include diodes, power transistors, IGBTs, and GTOs, optoelectronic circuits, circuits subject to single event upset, thin film transistor circuits, high-frequency circuits, precision analog circuits, and high performance digital circuits.

MIXEDMODE circuits can include up to 200 nodes, 300 elements, and up to ten numerical simulated ATLAS devices. These limits are reasonable for most applications. But, they can be increased in custom versions on request to Silvaco. The circuit elements that are supported include dependent and independent voltage and current sources as well as resistors,capacitors, inductors, coupled inductors, MOSFETs, BJTs, diodes, and switches. Commonly used SPICE compact models are available. The SPICE input language is used for circuit specification.

This chapter describes circuit simulation capabilities rather than device simulation capabilities. The first part of the chapter contains introductory and background information. Then, describes presents and explains MIXEDMODE syntax. This is followed by some sample input decks. The final sections contain a statement reference and a detailed description of the provided electrical compact models for diodes, BJTs, and MOSFETs.

4.3.2 Background

Circuit simulators such as SPICE solve systems of equations that describe the behavior of electrical circuits. The devices that are of interest to circuit designers are normally well characterized. Compact or circuit models are analytic formulae that approximate measured terminal characteristics. Advanced compact models provide high accuracy with minimum computational complexity. Device modeling, device characterization and parameter extraction are concerned with the development and use of accurate and efficient compact models.

Physically based device simulation solves systems of equations that describe the physics of device operation. This approach provides predictive capabilities and information about the conditions inside a device. It can, however, require significant amounts of CPU time. Information is usually transferred from device simulation to circuit simulation as follows: electrical characteristics are calculated using a physically-based device simulator. These calculated electrical characteristics are then used as input by a device modeling and parameter extraction package such as UTMOST. The extracted parameters are used to characterize a compact model used by the circuit simulator. This approach is adequate for many purposes but has limitations. It requires that satisfactory compact models already exist. The use of compact models always introduces some error. Models that are adequate for digital circuit simulation may be inadequate for other applications. Applications and devices for which compact modeling is not always satisfactory include: precision low power, high power, high frequency circuit simulation, SOI, IGBT, GTO, TFT, and optoelectronic devices.

4.3.3 Advantages of MixedMode Simulation

The limitations of compact models can be overcome by using physically-based device simulation to predict the behavior of some of the devices contained in a circuit. The rest of the circuit is modeled using conventional circuit simulation techniques. This approach is referred to as mixedmode simulation, since some circuit elements are described by compact models, and some by physically-based numerical models. MIXEDMODE simulation provides several worthwhile advantages. No compact model need be specified for a numerical physically-based device. The approximation errors introduced by compact models can be avoided particularly for large signal transient performance. You can also examine the internal device conditions within a numerical physically-based device at any point during the circuit simulation. But the cost is increased CPU time over SPICE as CPU time is comparable to a device simulation excluding the external circuit nodes. MIXEDMODE simulation normally uses numerical simulated devices typically only for critical devices. Non-critical devices are modeled using compact models.

4.4 ATLAS and SPICE Simulated NMOS:

In MIXEDMODE Simulation first of all a NMOS device is designed which is Recessed Channel MOSFET using ATLAS, thereafter a standard NMOS which is SPICE Simulated used in implementation of NAND gate by adjusting proper bias voltage and threshold voltage.

4.4.1 ATLAS Simulated NMOS:

Recessed Channel MOSFET has the drain and source regions which are separated from one another through a groove, the extension of the drain electric field toward the channel region is restrained. Thus, the presence of groove minimizes the SCEs and punch through effects, thereby enhancing the hot-carrier reliability.

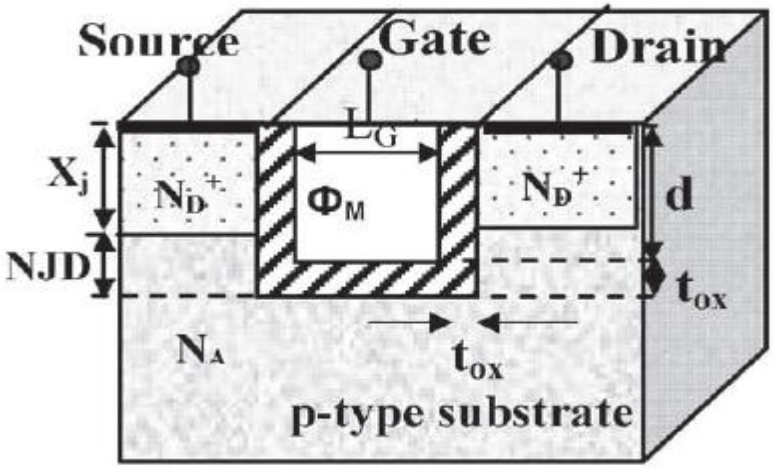


Fig. 4.7 *Schematic cross-sectional view of Recessed Channel MOSFET*

In this structure, two potential barriers are formed at the corners, referred to as the "corner effect," due to the high density of electric field lines at the corners, which leads to SCE immunity. Furthermore, as the negative junction depth (NJD) increases (or the source/drain junction depth decreases), the potential barriers augment. The carrier velocity thus goes down, causing the drain current driving capability to degrade. Moreover, the charge carriers now require high energy to surmount the potential barriers, thereby raising the device's threshold voltage.

In the simulation for sub-50-nm gate length devices, the drift-diffusion model is not acceptable since it ignores the nonlocal transport of carriers and the carrier heating. In our simulation, we have adopted the hydrodynamic energy transport model which includes the continuity equations, momentum transport equations, energy balance equations of the carriers, and the Poisson equation. It can model the nonlocal transport phenomenon and is more accurate than the drift-diffusion method. In the study of gate and substrate currents, the impact ionization and hot-electron-injection models are used to provide an accurate measure of hot-carrier-injection fluxes in short channel MOS technologies.

All the simulations have been performed using physical models accounting for the electric field-dependent and concentration-dependent carrier mobilities, **Shockley–Read–Hall** recombination/generation with doping dependent carrier lifetime, and Auger recombination.

The mobility model used is the inversion layer **Lombardi CVT** mobility model, wherein concentration-dependent mobility, high field saturation model, and mobility degradation at interfaces are all included [56]. Default simulator coefficients for all parameters have been employed. In order to fairly analyze the device performances, all the four devices are optimized to have the same threshold voltage, i.e., 0.3 V, and comparisons are then made to give a fair insight into the effectiveness of various RC designs.

Moreover, normalization of the *x*-axis has been done to give a fair comparison of various structural parameter variations on the device performance. This is because by changing the gate length and NJD, the effective channel length [54] would change, and as a result, the position along the channel will also vary in comparison to other structural parameter variations.

TABLE 4.1

DEFAULT DESIGN PARAMETERS USED IN THE ANALYSIS FOR VARIOUS RC DEVICE DESIGNS

Design Parameters for RC Device Designs	
Channel Length (L_G=L_{G1}+L_{G2})	50nm (L_{G1}=L_{G2}=25nm)
Device Width (W)	1μm
Groove Depth, (d)	80nm
Source/Drain Junction Depth (X_j)	74nm
Negative Junction Depth (NJD)	10nm
Substrate Doping (N_A)	$1x10^{17}$ cm^{-3}
Source/Drain Doping (N_D^+)	$1x10^{20}$ cm^{-3}
Physical Oxide Thickness (t_{ox})	4nm (t_{ox1}=t_{ox2}=2nm)
Permittivity of SiO_2	ε_{ox}=ε_{ox1}=3.9
Permittivity of High-K	ε_{ox2}=10
Effective Oxide Thickness (EOT)	$EOT = t_{ox1} + \frac{\varepsilon_{ox1}}{\varepsilon_{ox2}} t_{ox2}$
Substrate Bias (V_{SUB})	0V
Drain Bias (V_{DS})	1V
For RC & MLaG-RC MOSFETs	Work function (ϕ_{M1}) = 4.77V
For GEWE-RC & MLGEWE-RC MOSFETs	Workfunction (ϕ_{M1}) = 4.77V & (ϕ_{M2}) = 4.10V.
The design parameters, as discussed above, are the default parameters used in the analysis, unless otherwise stated.	

4.4.2 RESULTS :

(a) ATLAS Designed Recessed Channel MOSFET:

We are considering above design parameters and choosing appropriate mobility and energy transport models thus the structure designed is as given below-

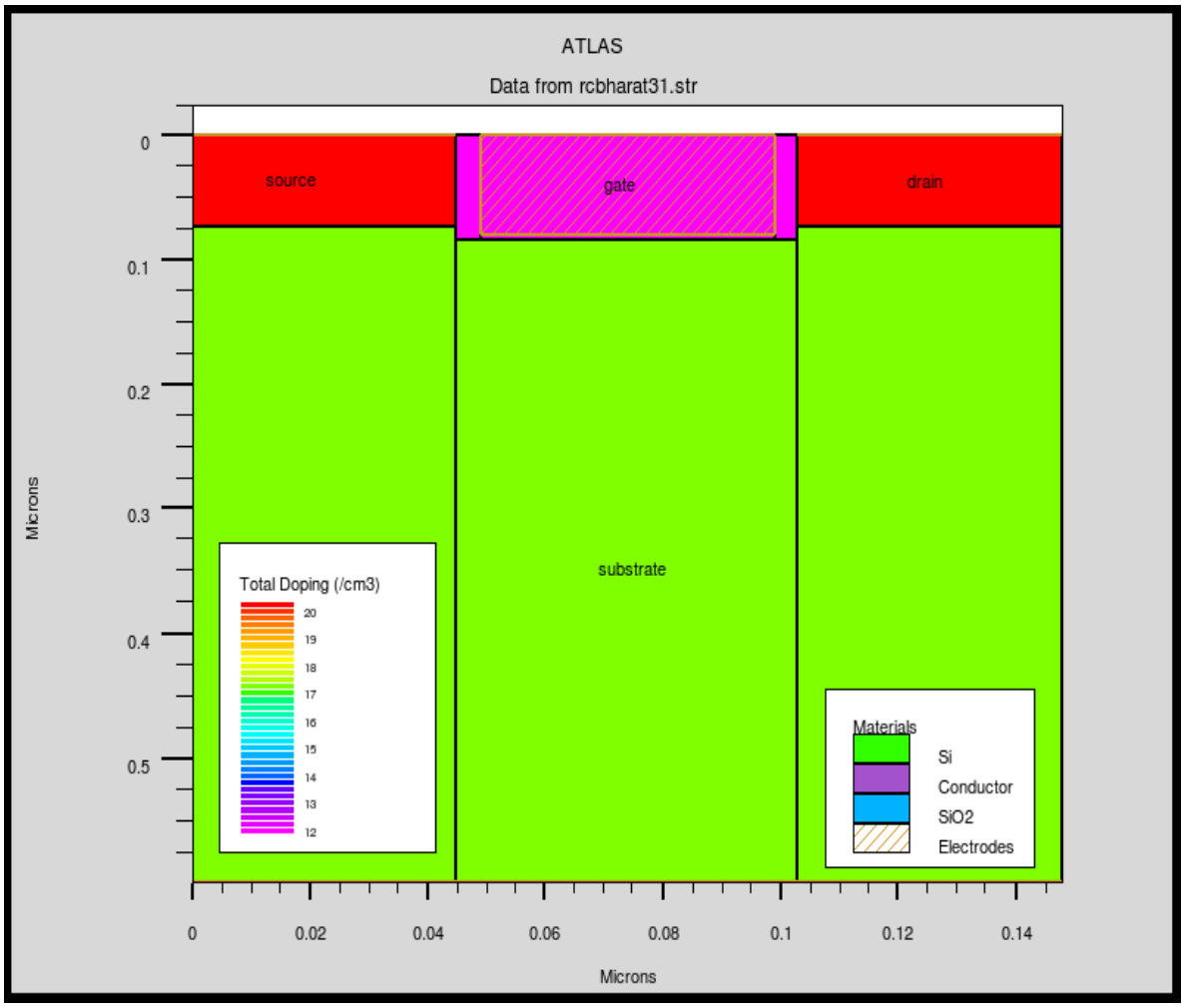


Fig. 4.8 *ATLAS Simulated Recessed Channel MOSFET*

(b) Gate Voltage v/s Drain Current Characteristics:

Gate Voltage v/s Drain Current curve gives the information that threshold voltage is 0.5 volt that is further used in proper biasing of both NMOS structures used in NAND gate design.

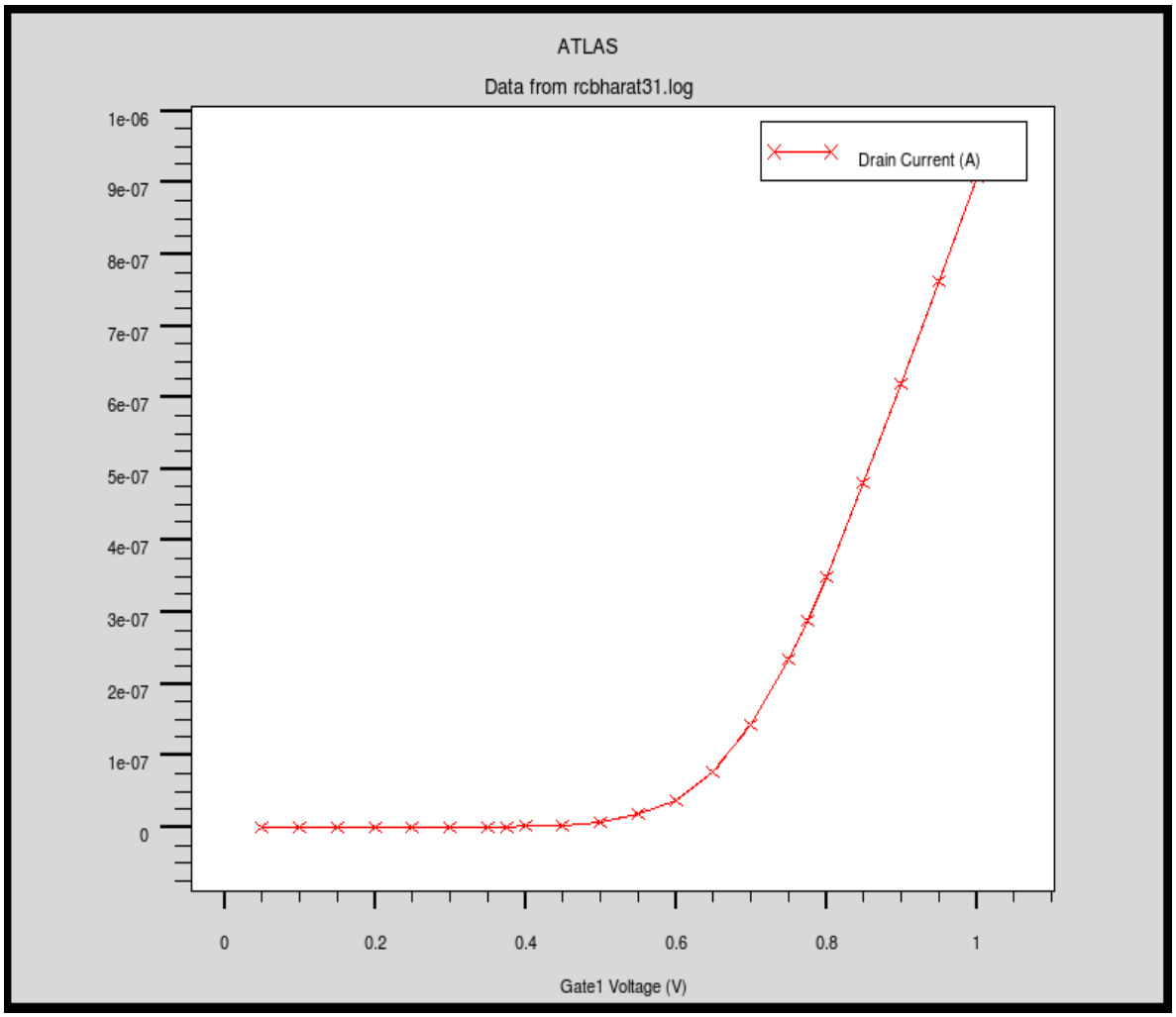


Fig 4.9 *Gate Voltage v/s Drain Current Characteristics*

(c) SPICE Simulated Standard NMOS:

Here in the simulation we are using Standard NMOS which is defined in SPICE library file having parameters as follows-

(1) Oxide thickness t_{ox}=0.02e-6

(2) Threshold Voltage=0.5v

(d) Transient Simulation for NAND gate Design:

In our Simulation ATLAS designed RC-MOSFET NMOS Structure is used as input file and is connected in proper way with SPICE Simulated NMOS for design of NAND gate which is further used as a Sub Circuit in Half Adder implementation because NAND is universal logic gate. Circuit configuration for NAND gate is as follows-

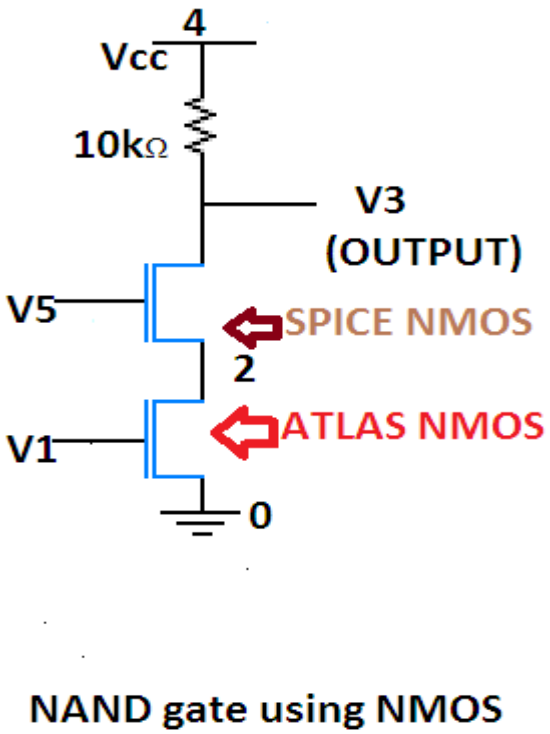
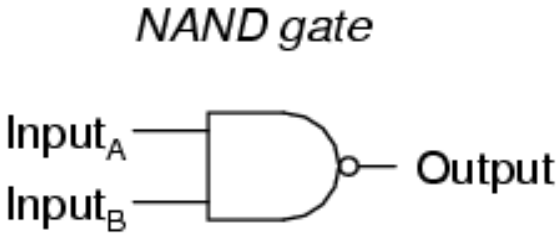


Fig 4.10 *NAND gate based on MIXEDMODE Simulation*

In digital electronics, a **NAND gate** (**Negated AND** or **NOT AND**) is a logic gate which produces an output that is false only if all its inputs are true. A LOW (0) output results only if both the inputs to the gate are HIGH (1); if one or both inputs are LOW (0), a HIGH (1) output results. It is made using transistors.

The NAND gate is significant because any boolean function can be implemented by using a combination of NAND gates. This property is called functional completeness.Digital systems employing certain logic circuits take advantage of NAND's functional completeness.



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

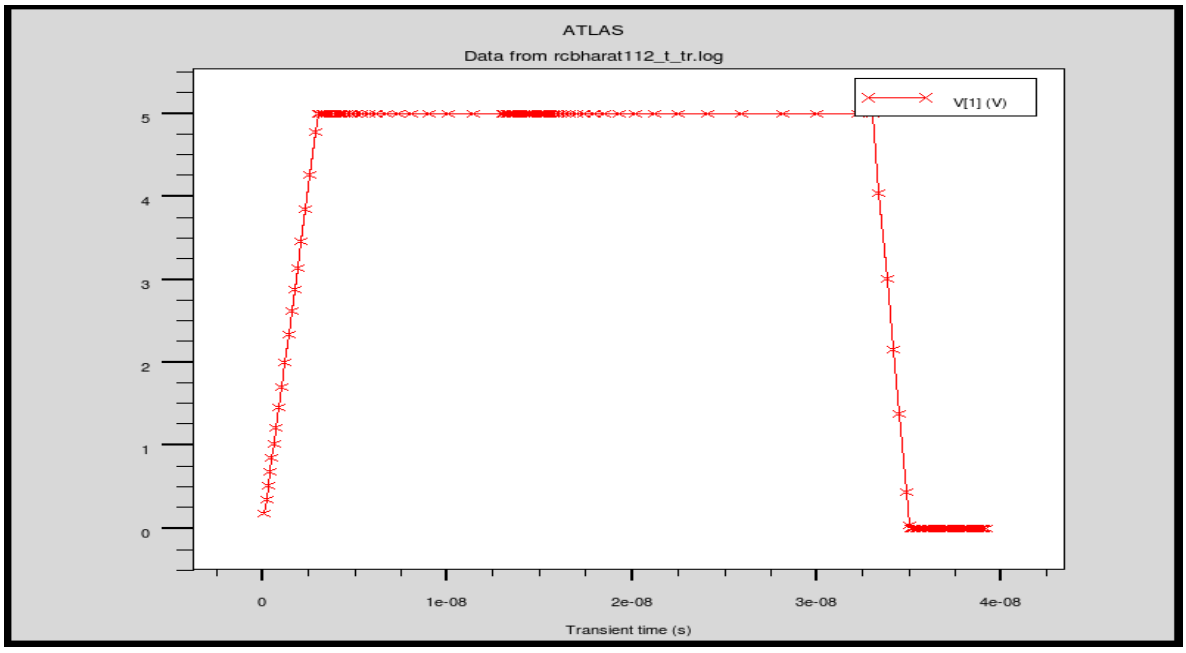
Fig 4.11 *Truth Table for NAND gate*

Now we concludes that if there are two pulses of 5 volt each, having different duty cycles are applied as inputs in designed NAND gate as **V1** and **V5** and output pulse is obtained as **V3,** here '0' represents ground terminal and '4' represents Vcc (as above fig 4.10).

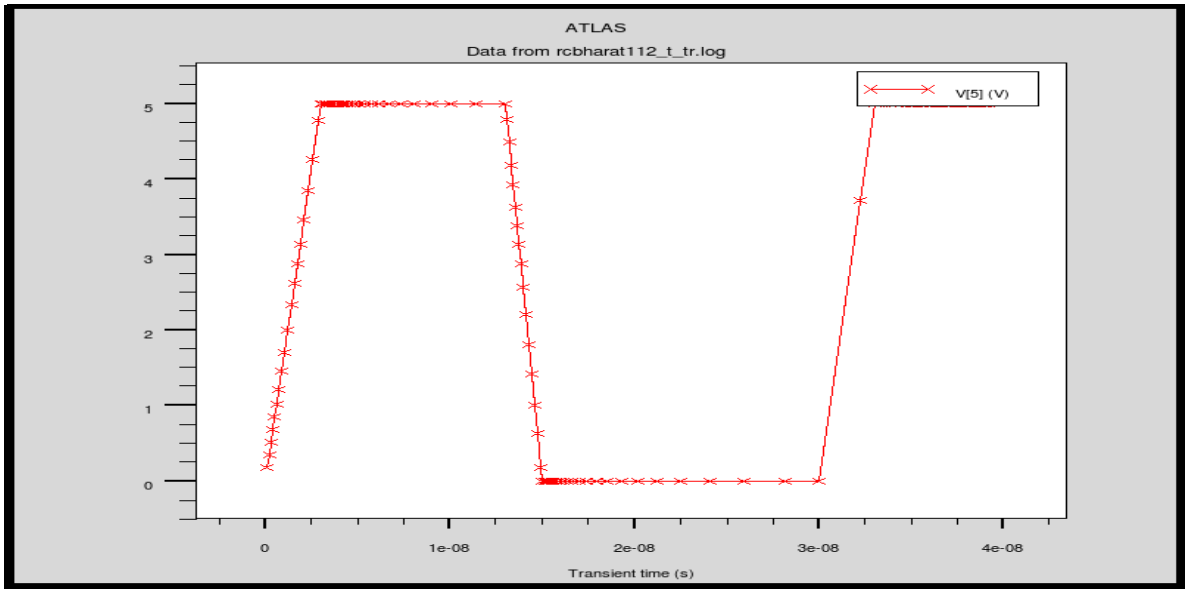
Transient curve Simulation gives the proper logic implementation for NAND gate as follows-

V1, V5 as input

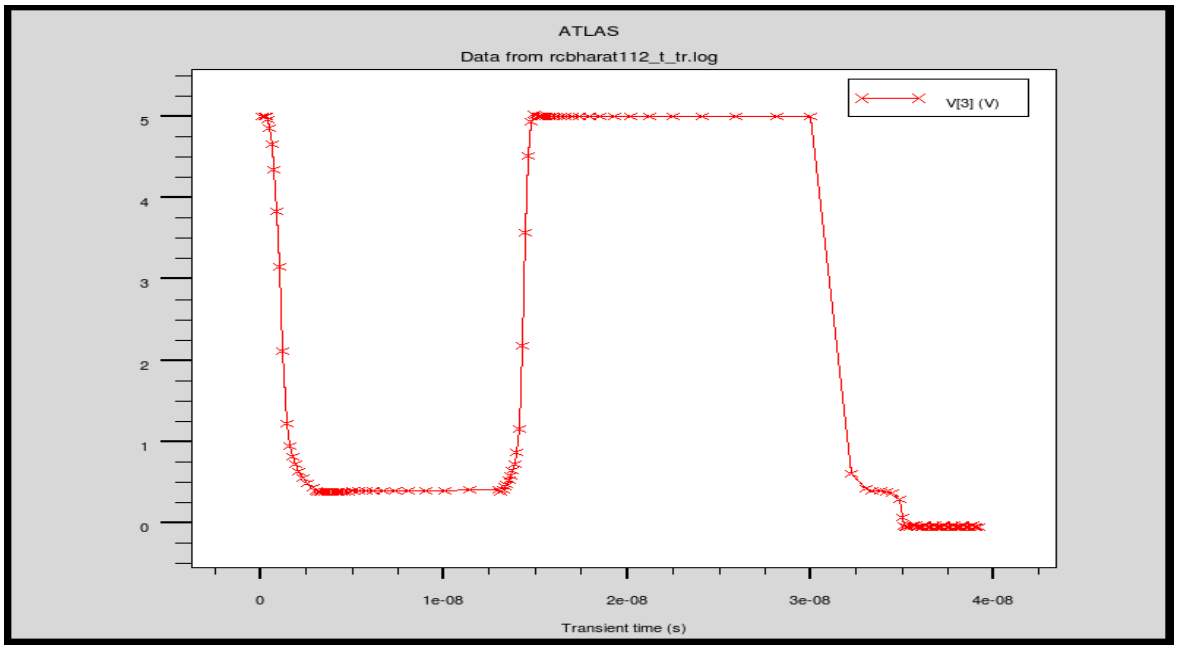
V3 as output



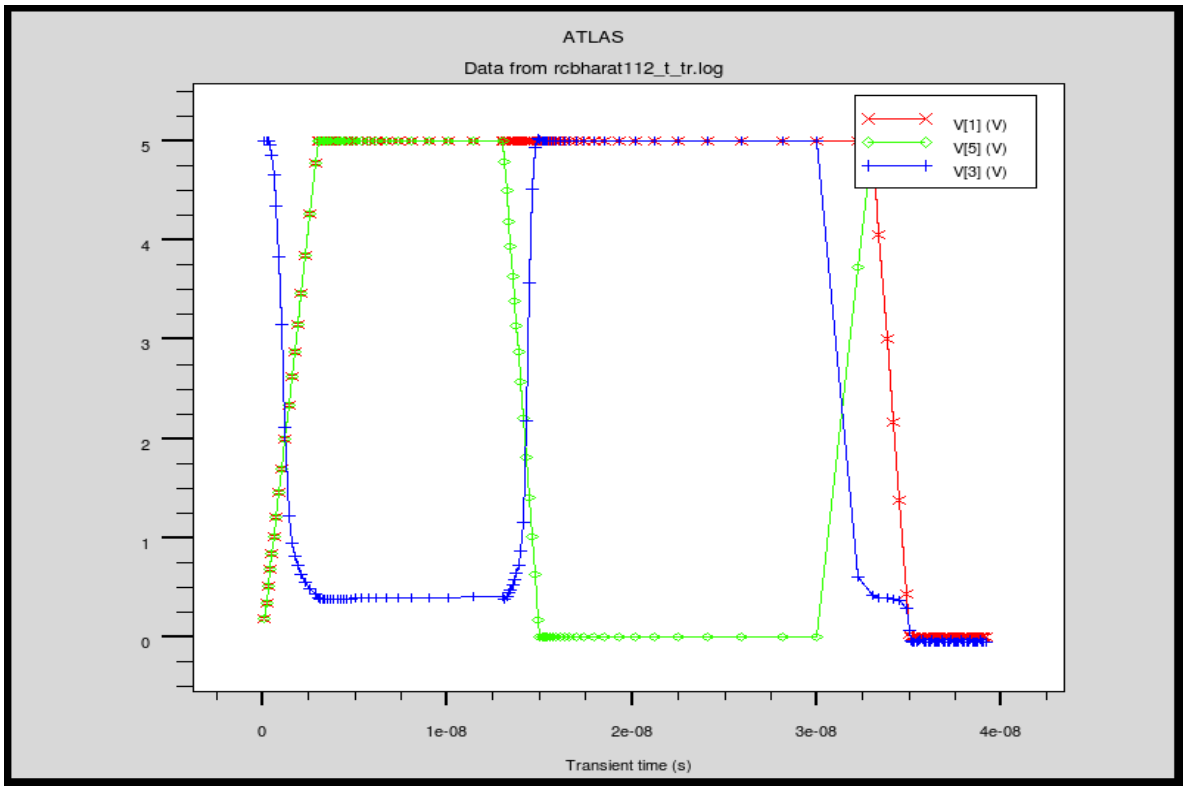
(a)



(b)



(c)



(d)

Fig 4.12 *(a)input V1 (b)input V5 (c)output V3 (d)all transient curves.*

Thus fig 4.12 concludes that NAND gate which is designed from MIXEDMODE simulation is proper working. Now such NAND gate is used as a Sub Circuit in SPICE code Simulation and Half Adder circuit is implemented as NAND is universal logic gate. Both SUM and CARRY expressions can be obtained, thus results should be displayed like below-

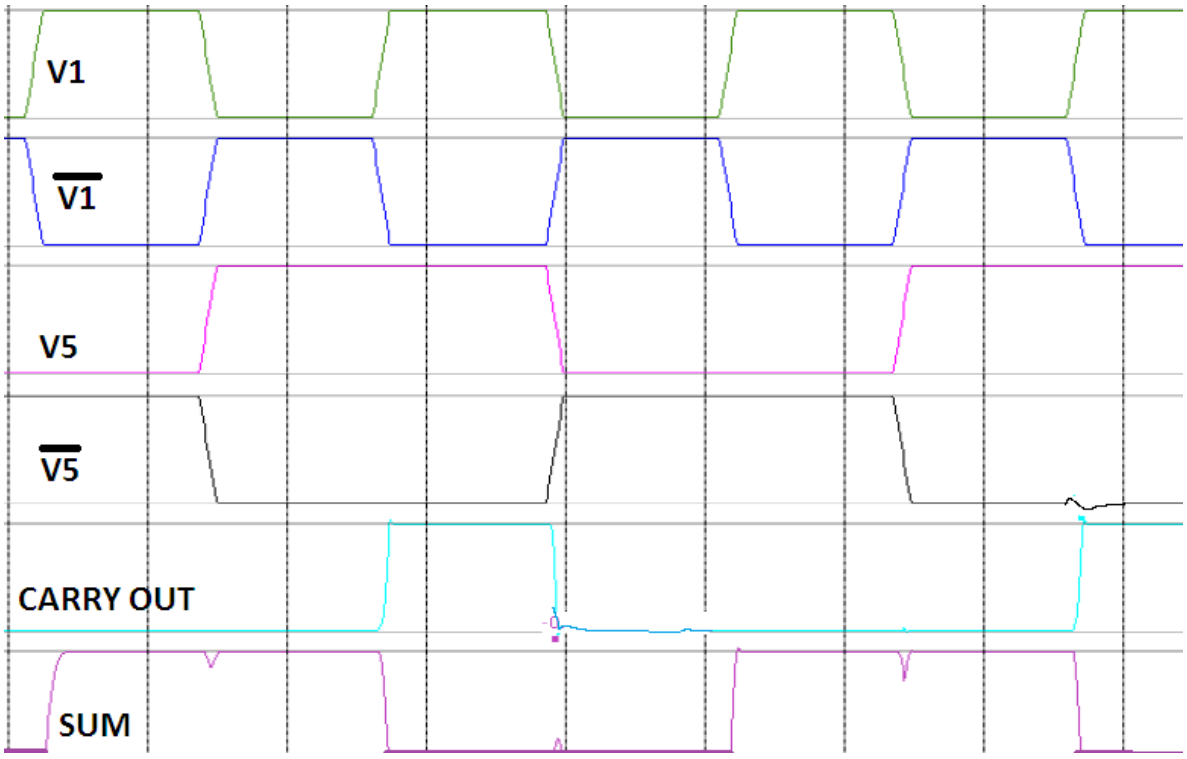


Fig 4.13 *Transient Plot for Half Adder Circuit*

Thus from simulation it is concluded that we can implement adder circuit by using two different NMOS transistors using MIXEDMODE simulation.

5. CONCLUSION AND FUTURE WORK:

We have studied Various parameters of Recessed Channel MOSFET i.e. oxide thickness, groove junction depth, gate dielectric etc. and thus performance is already evaluated in terms of DIBL, sub threshold voltage, impact ionization and thus device can be optimized.

In our simulation RC-MOSFET is designed so as to implement Half Adder Circuit using MIXEDMODE simulation because in comparison with conventional MOSFET, RC-MOSFET structure has better switching applications, there is improvement in terms of power dissipation and downscaling effects are also minimized, in a similar way Full adder circuit can also be implemented. Adder plays a very important role in arithmetic and logical calculations which can be further used in microcomputers.

In future there is a possibility of work in which low power adder circuit can be designed i.e. static and dynamic power dissipation of MOSFET can be lowered down by applying different engineering mechanism on MOSFET like different parameter variations of Recessed Channel MOSFET.

Thus there may be chance in future that a low power adder circuit that is designed can be fabricated with a proper method so as to optimize device performance.

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